

FIG. 1. (prior art)

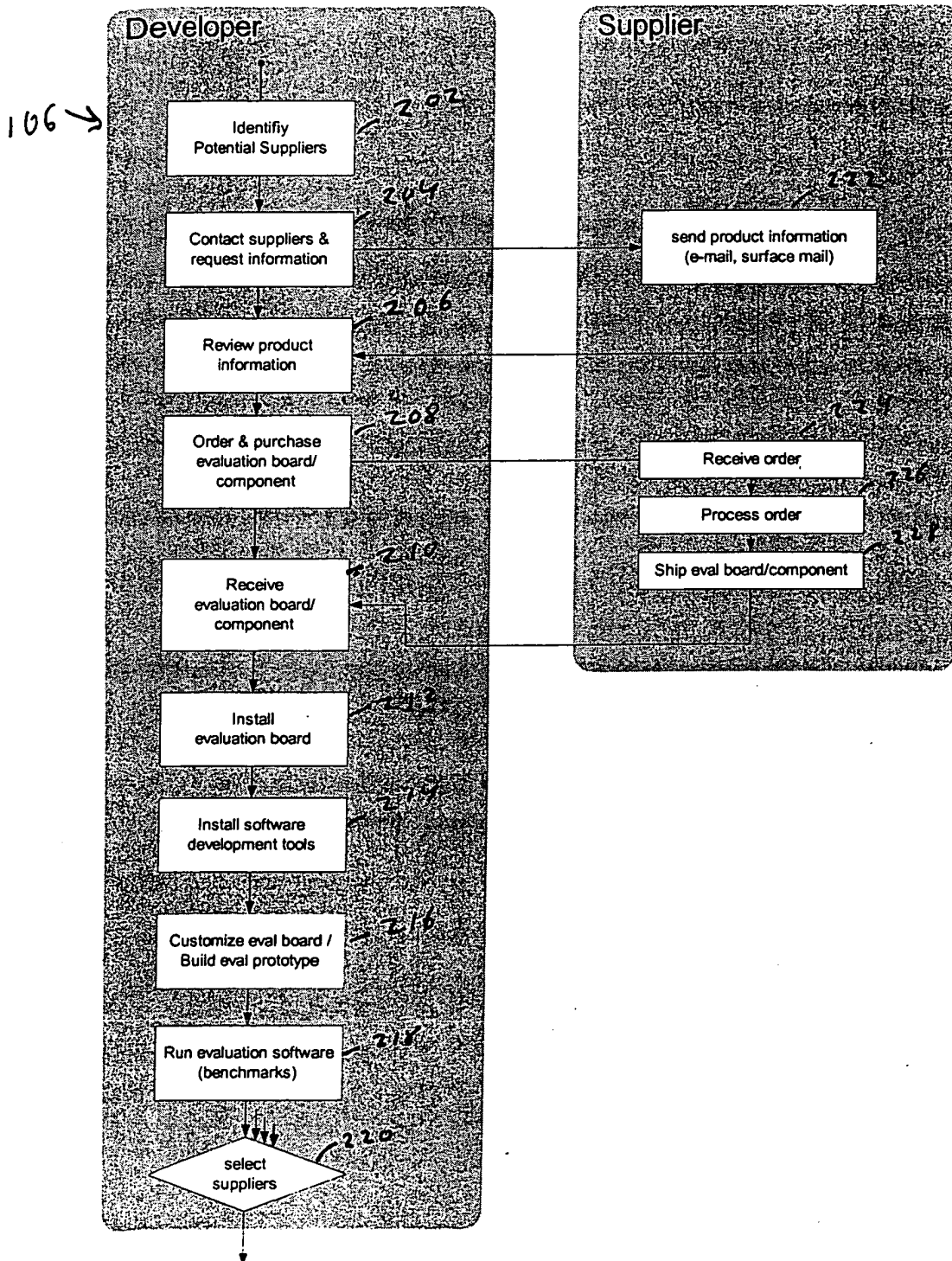
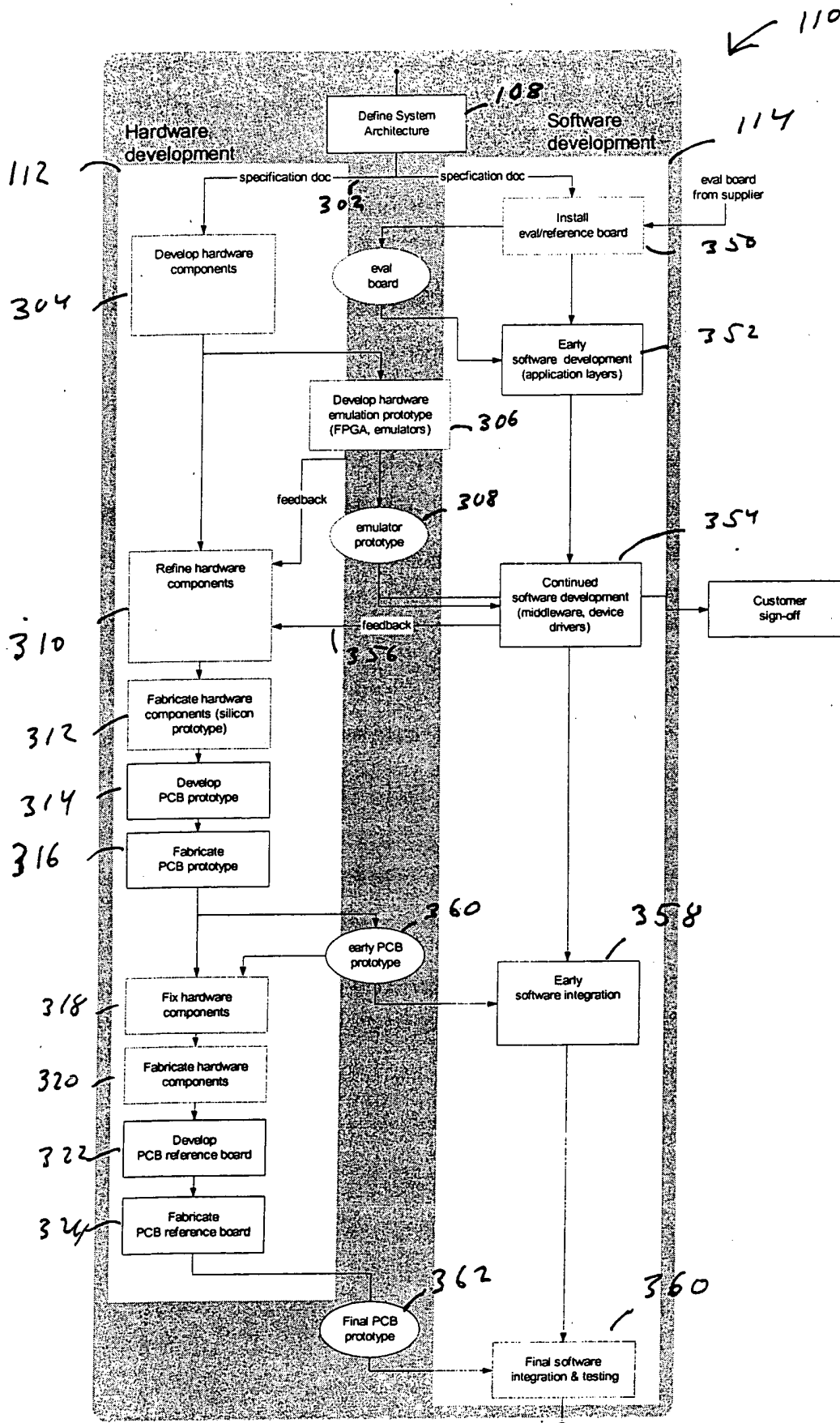


FIG. 2 (prior art)



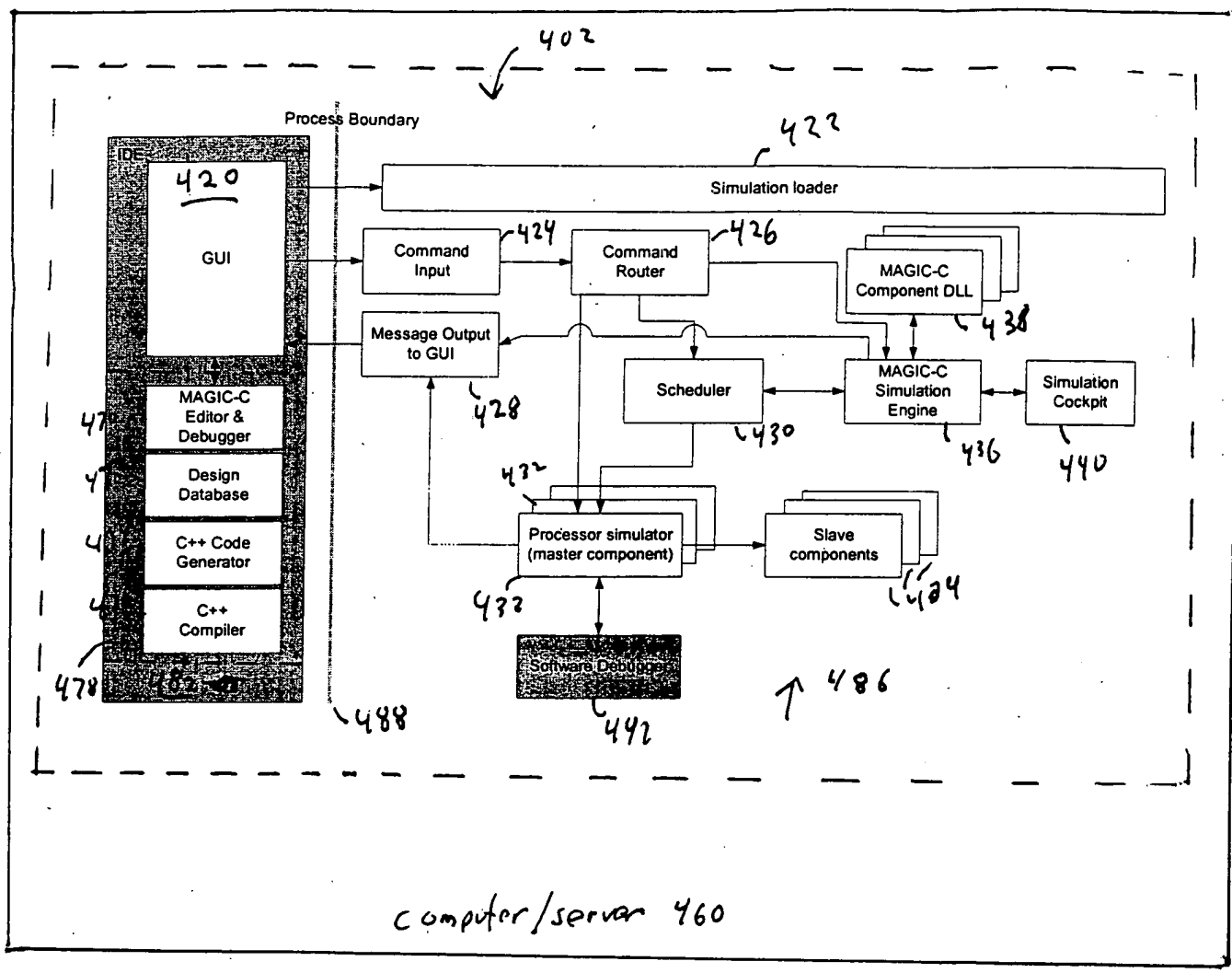


FIG. 4A

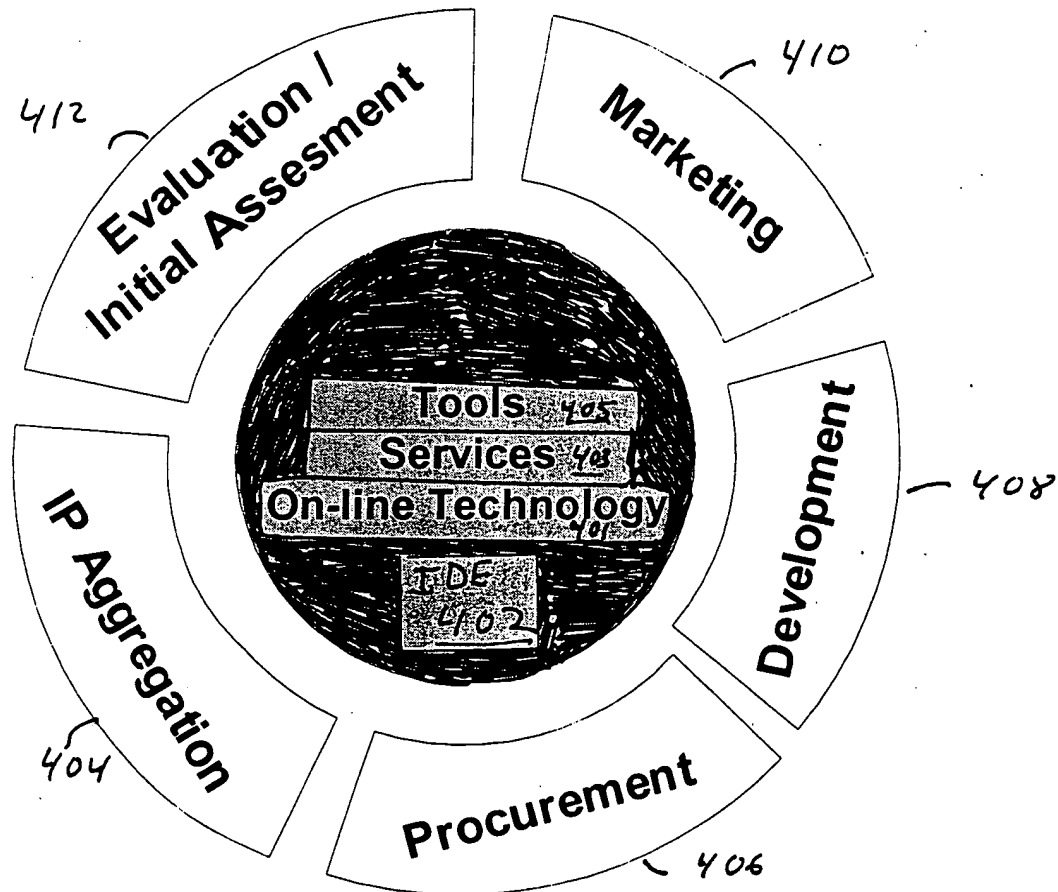


FIG. 4B

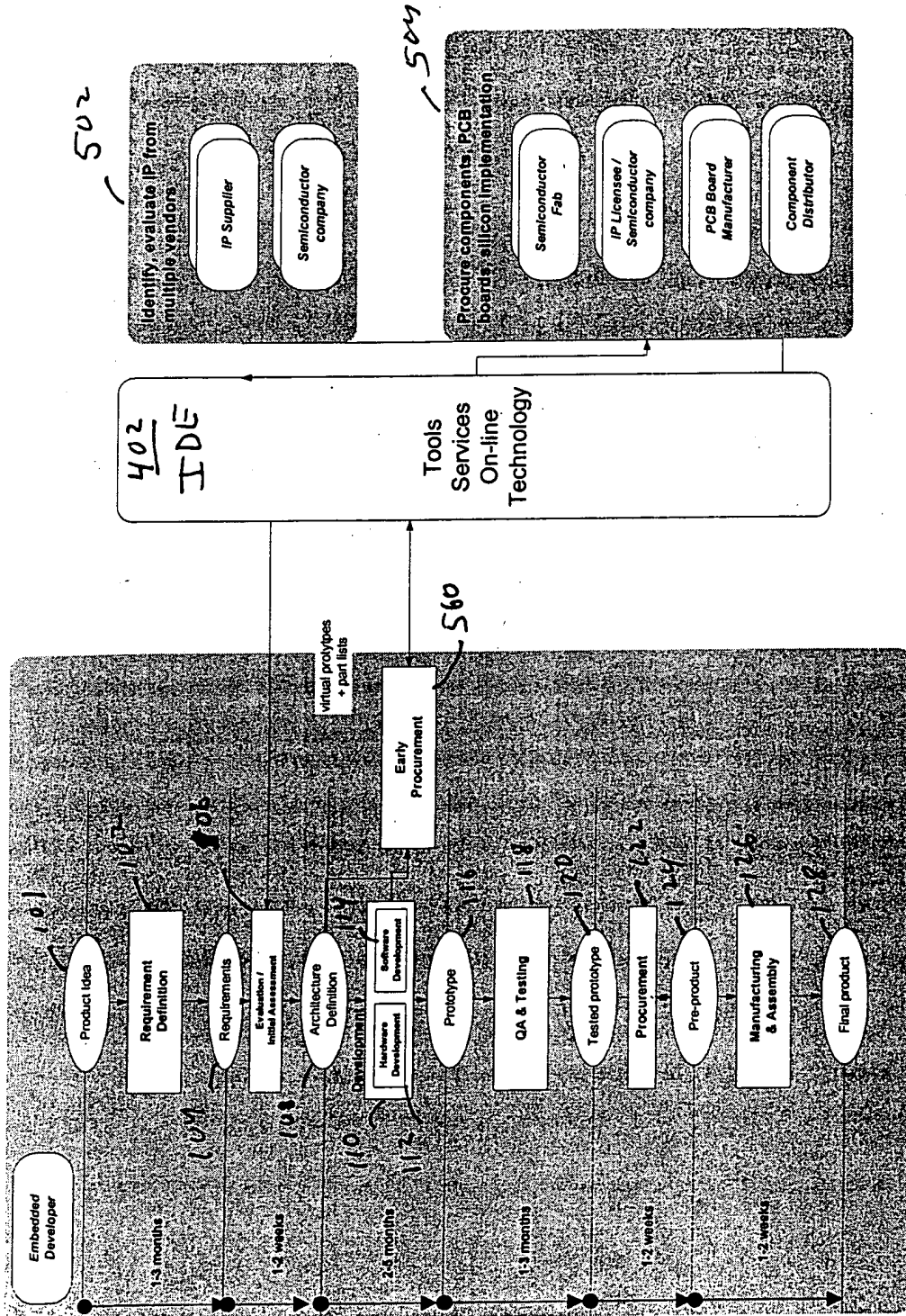


FIG. 5

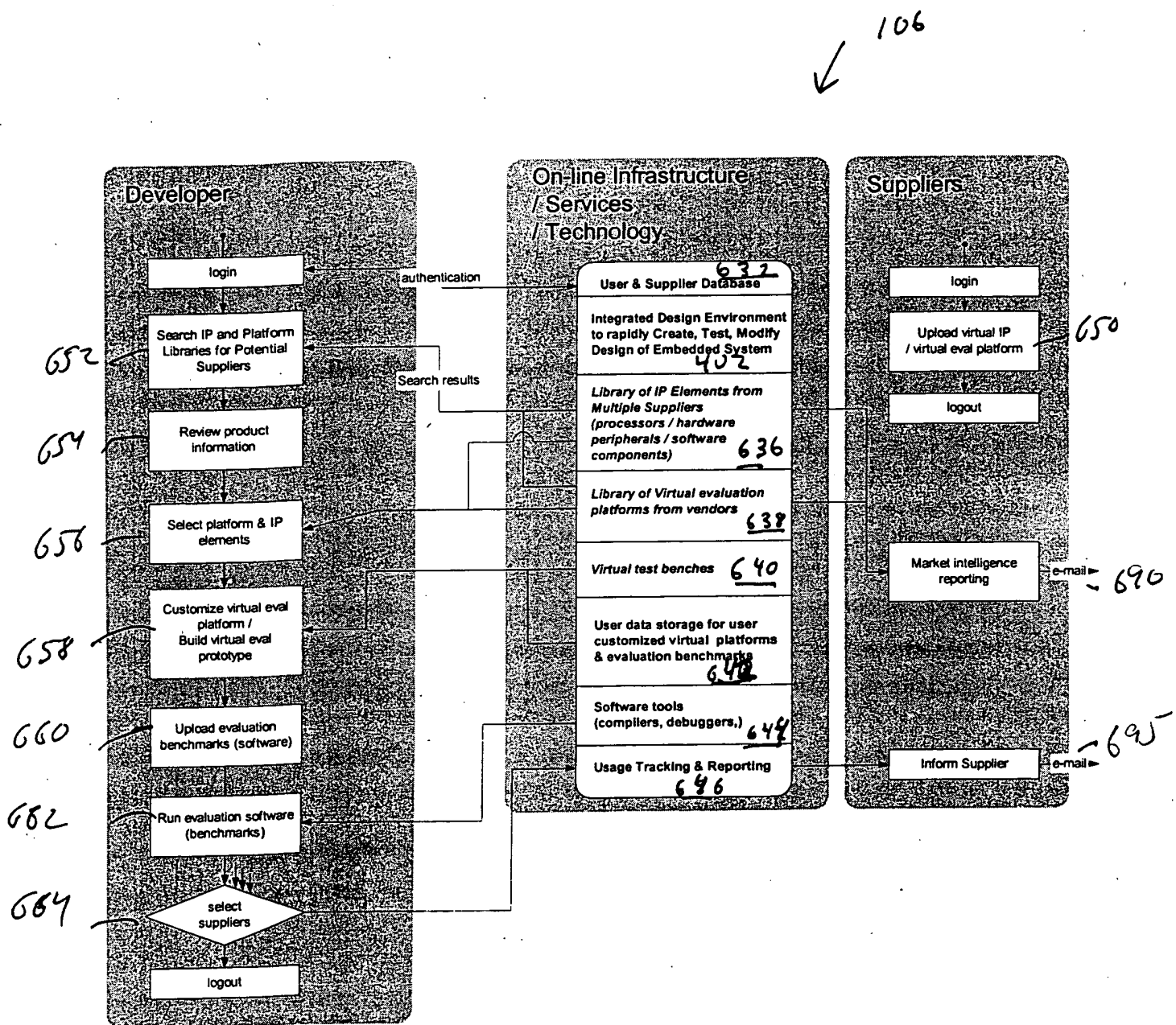


FIG. 6



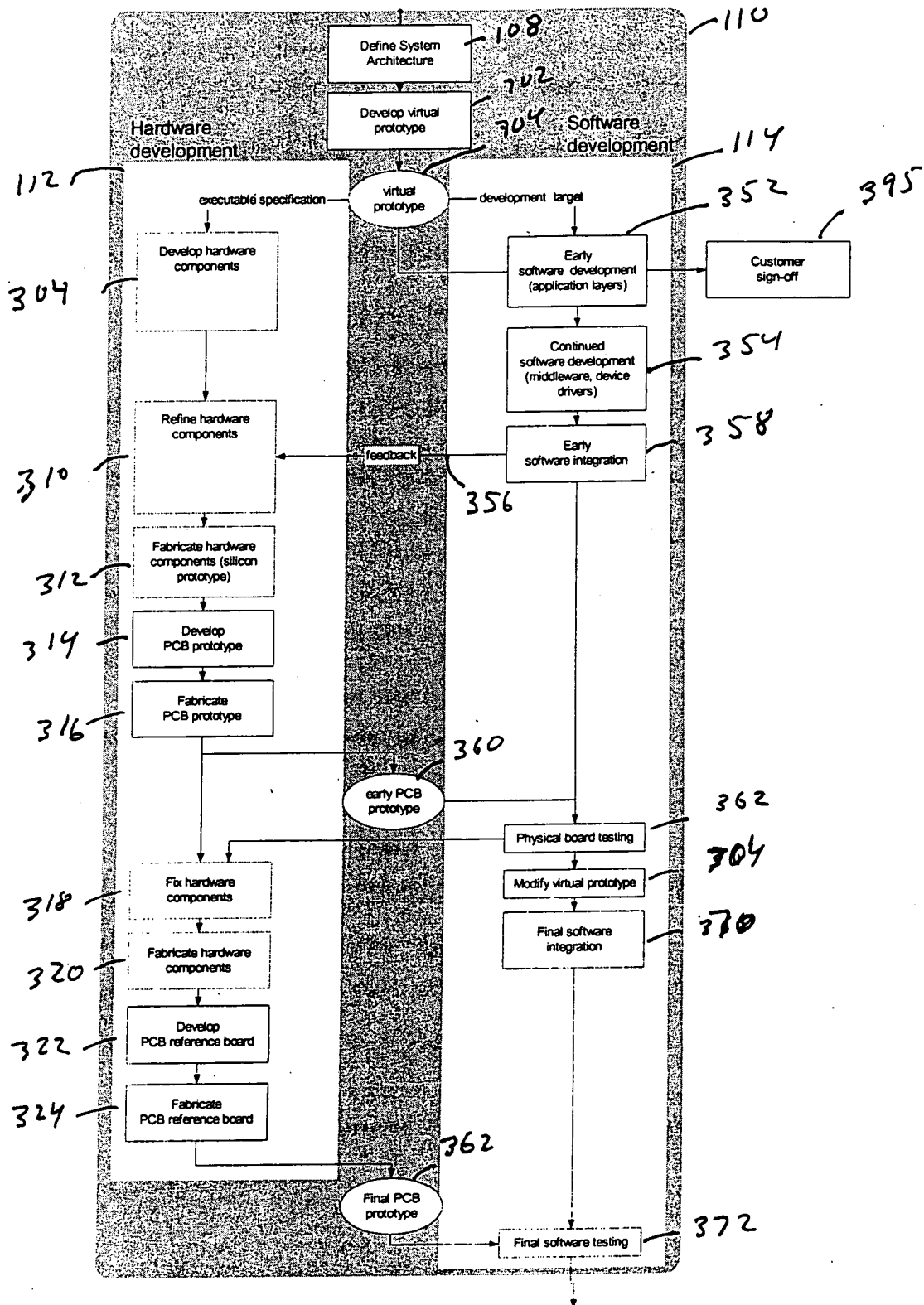


FIG. 7



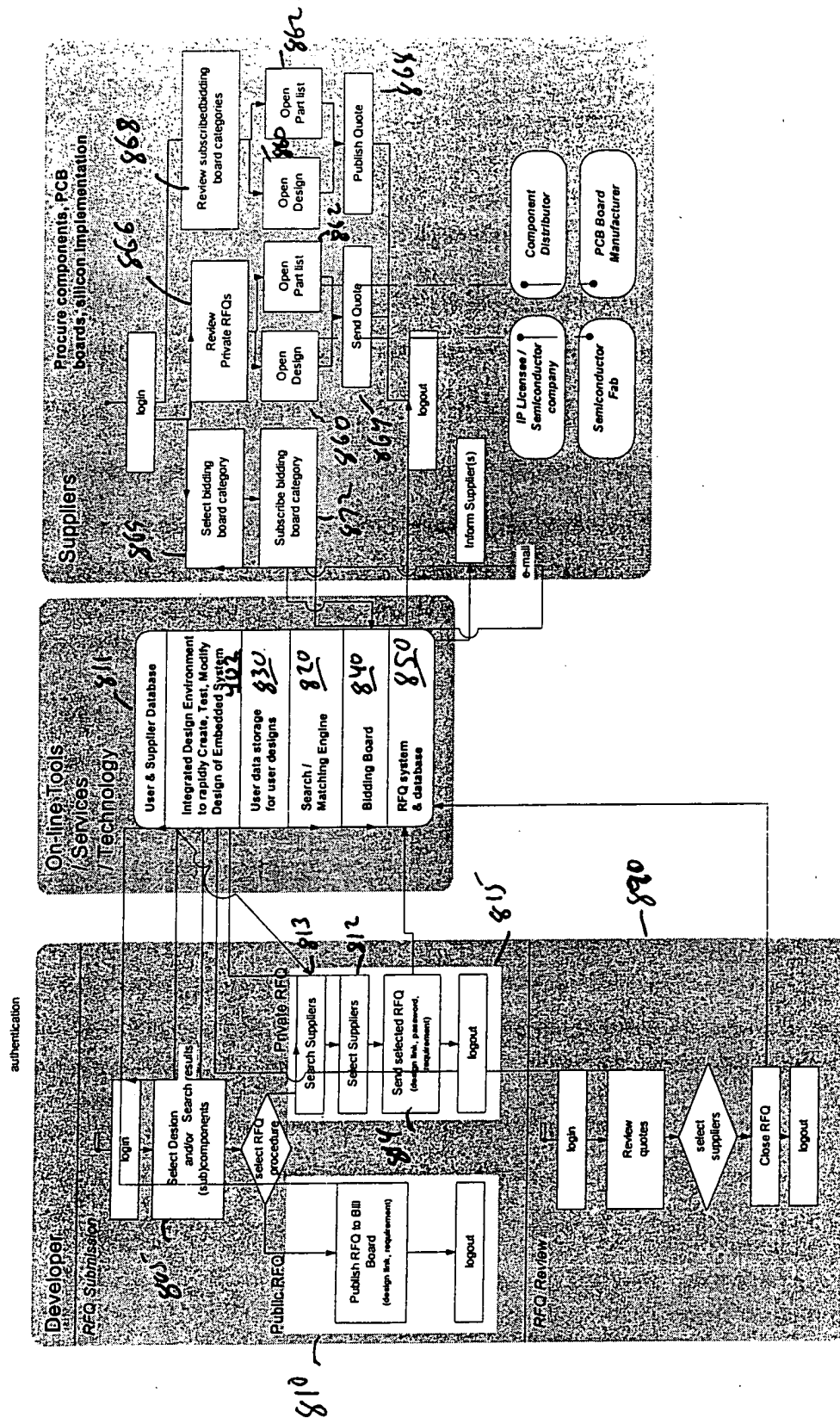


FIG. 8

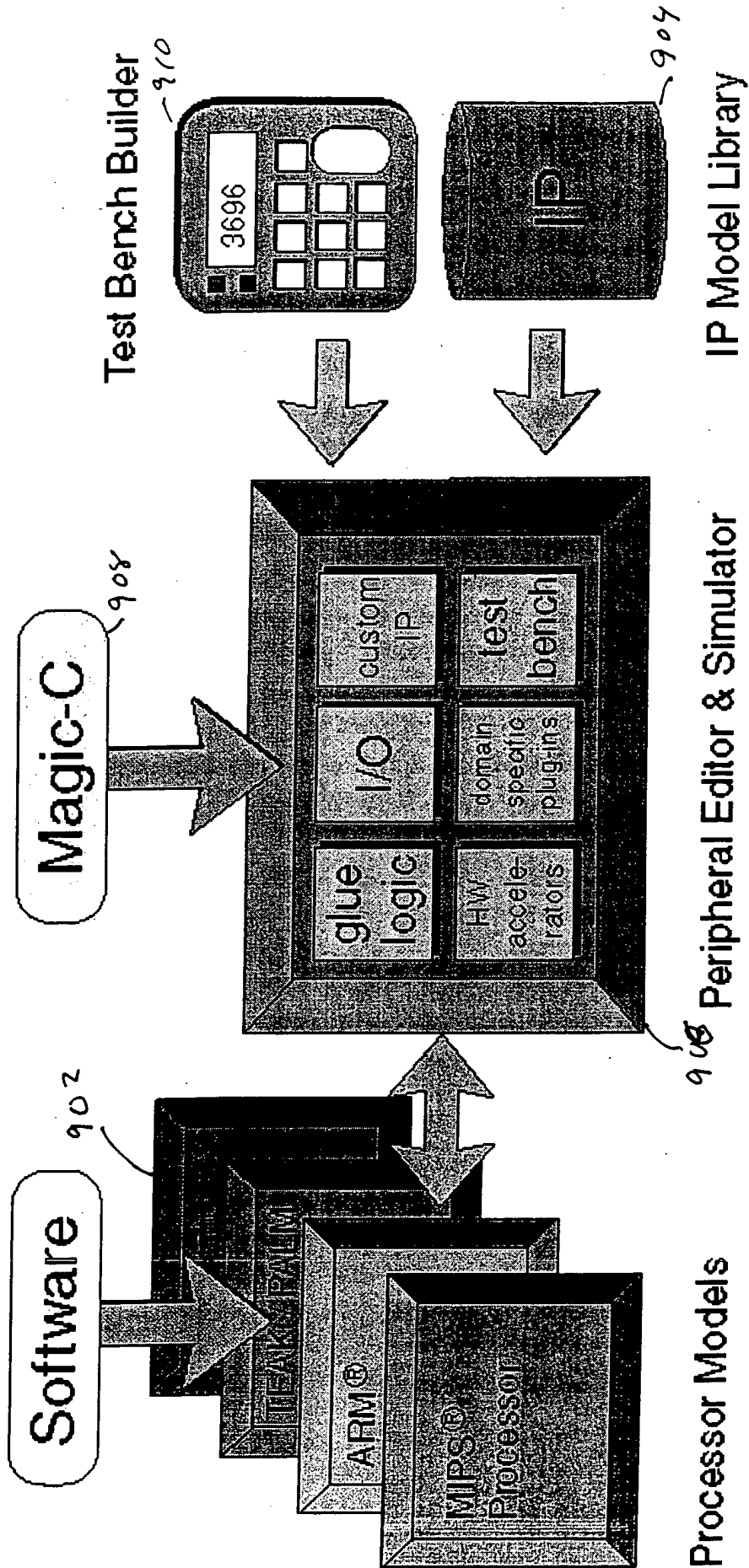


FIG. 9

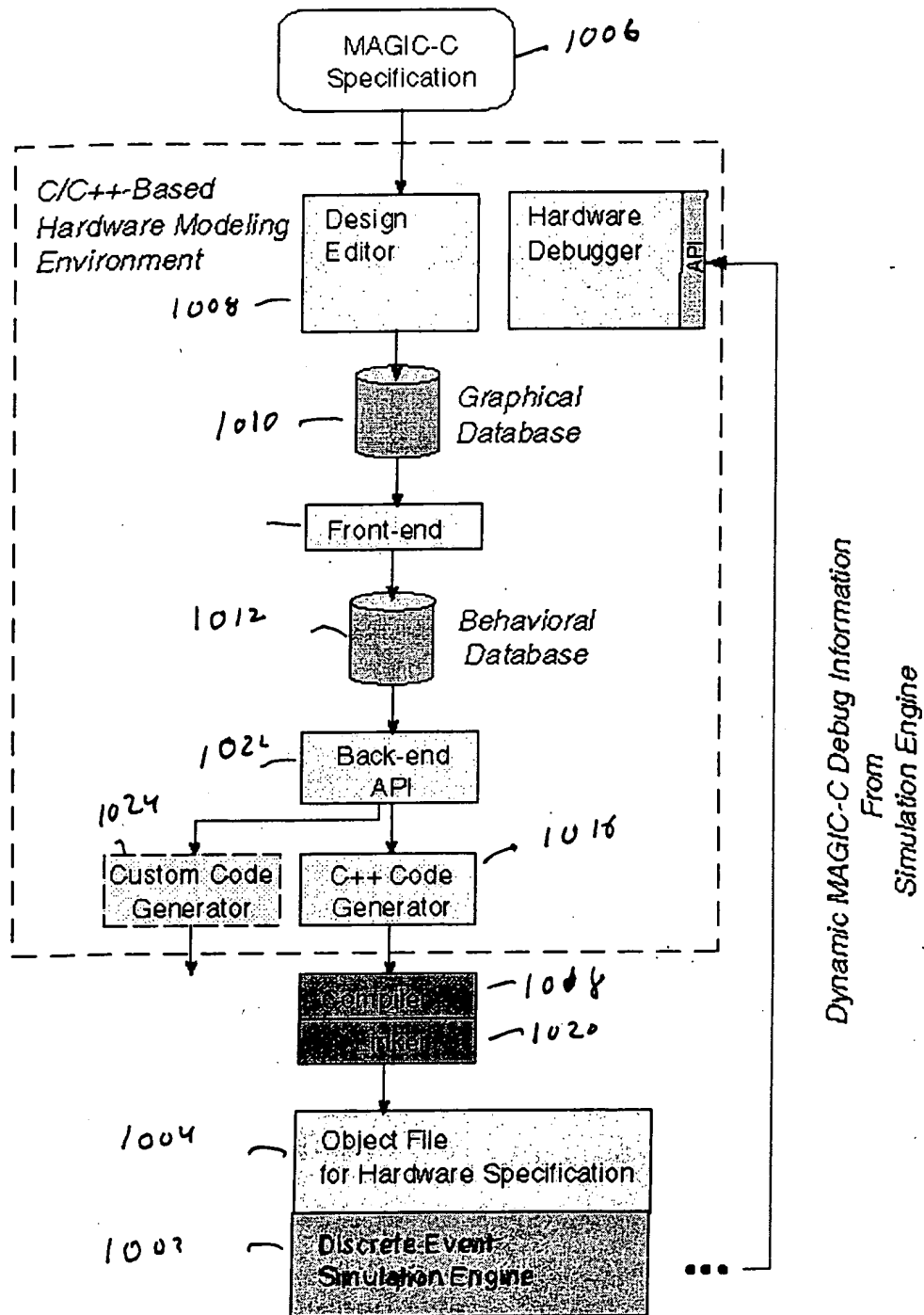


FIG. 10

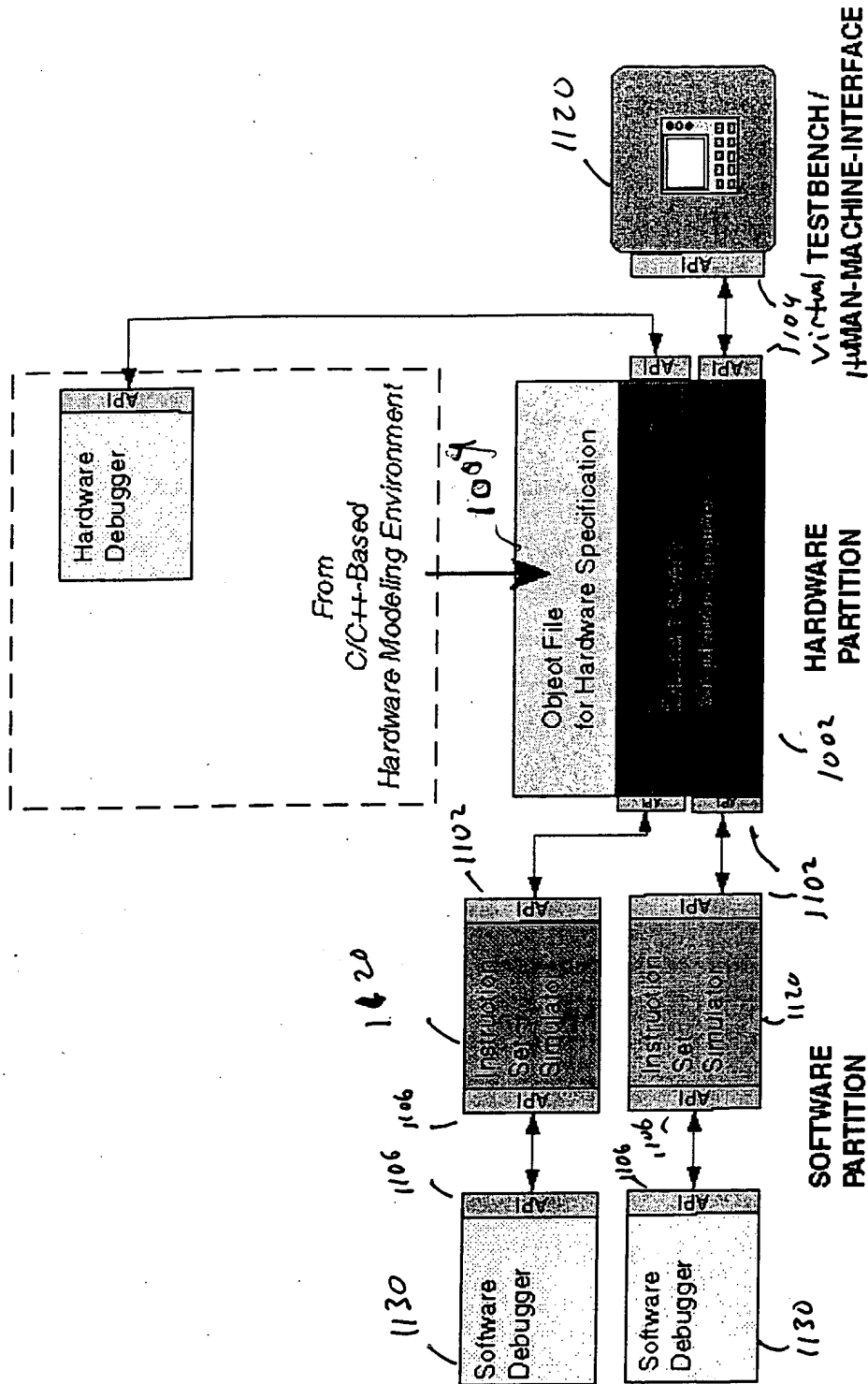


FIG. 11

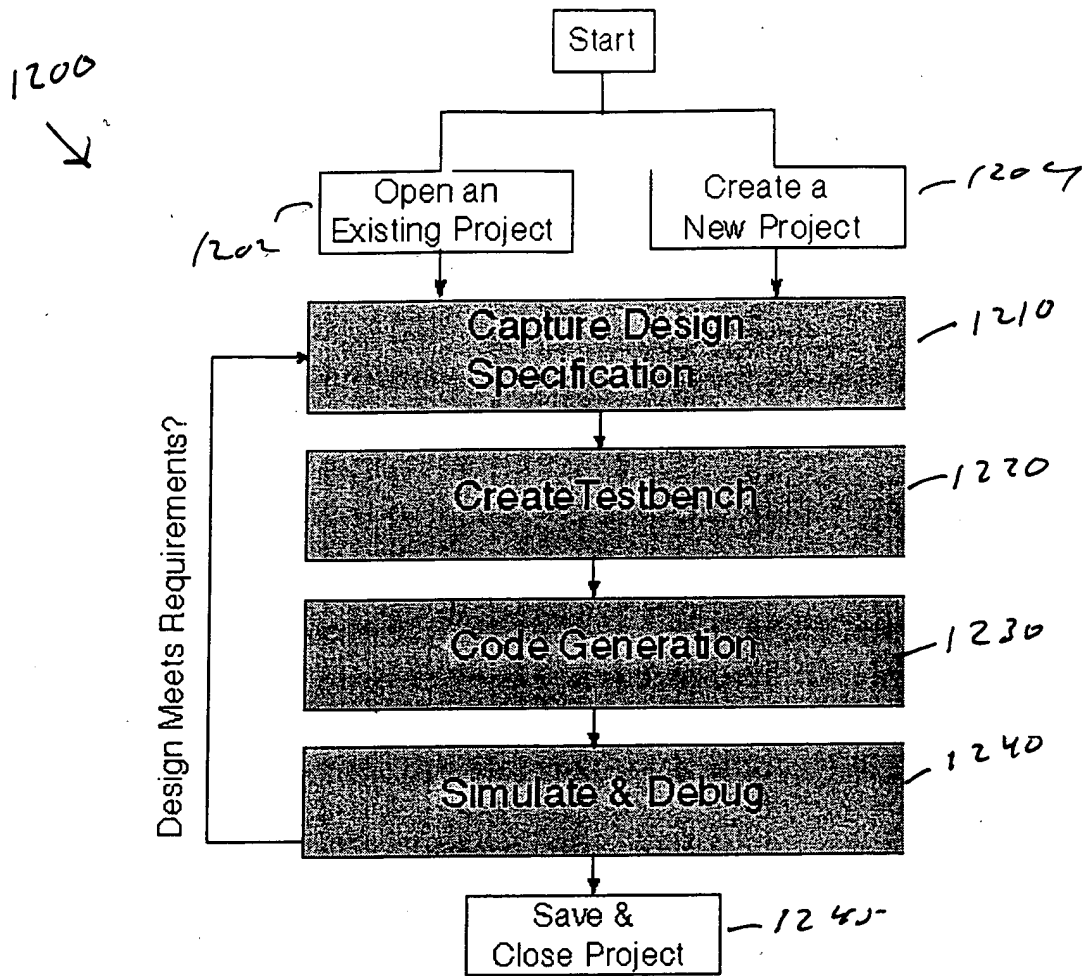


FIG. 12

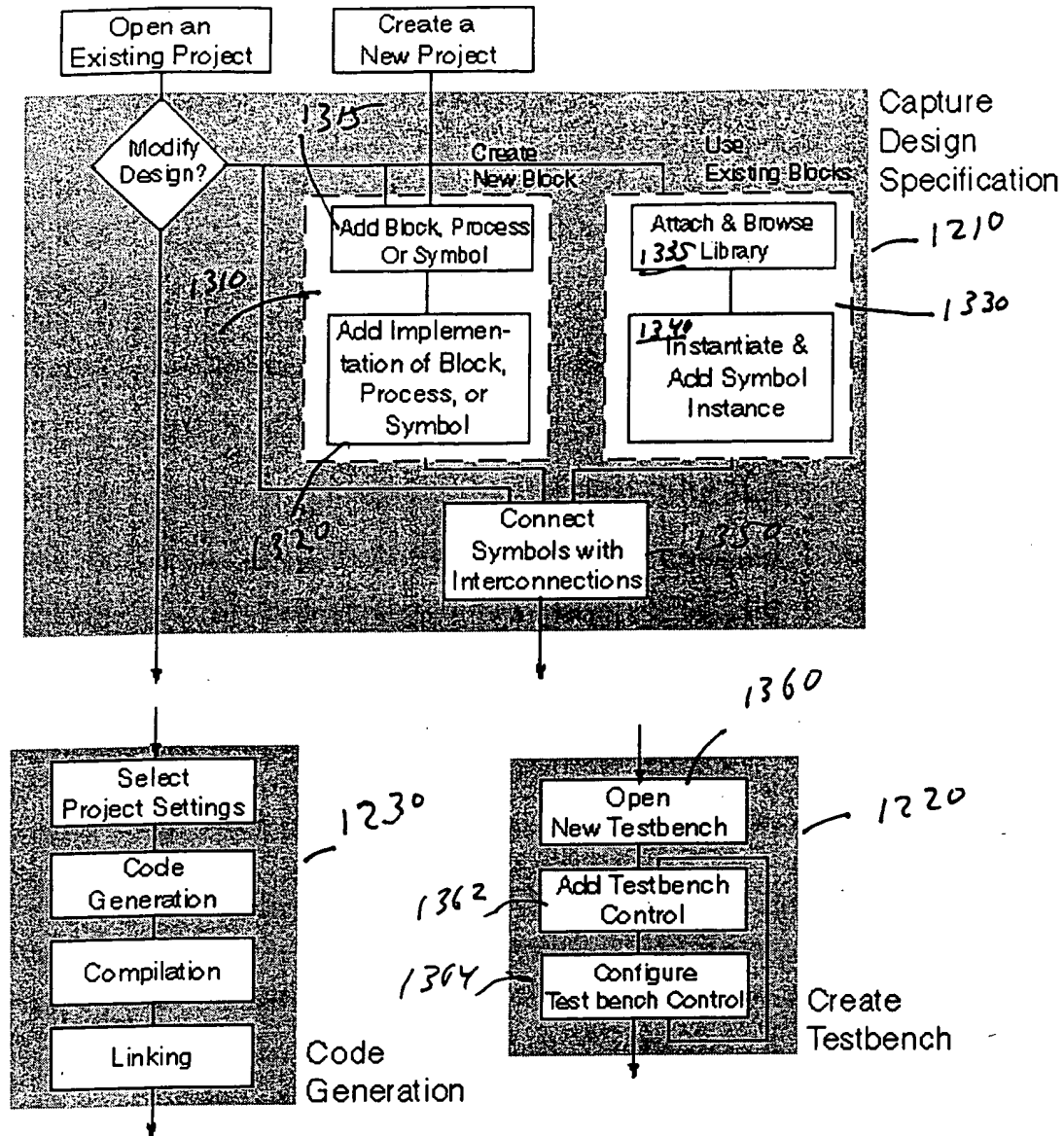


FIG. 13

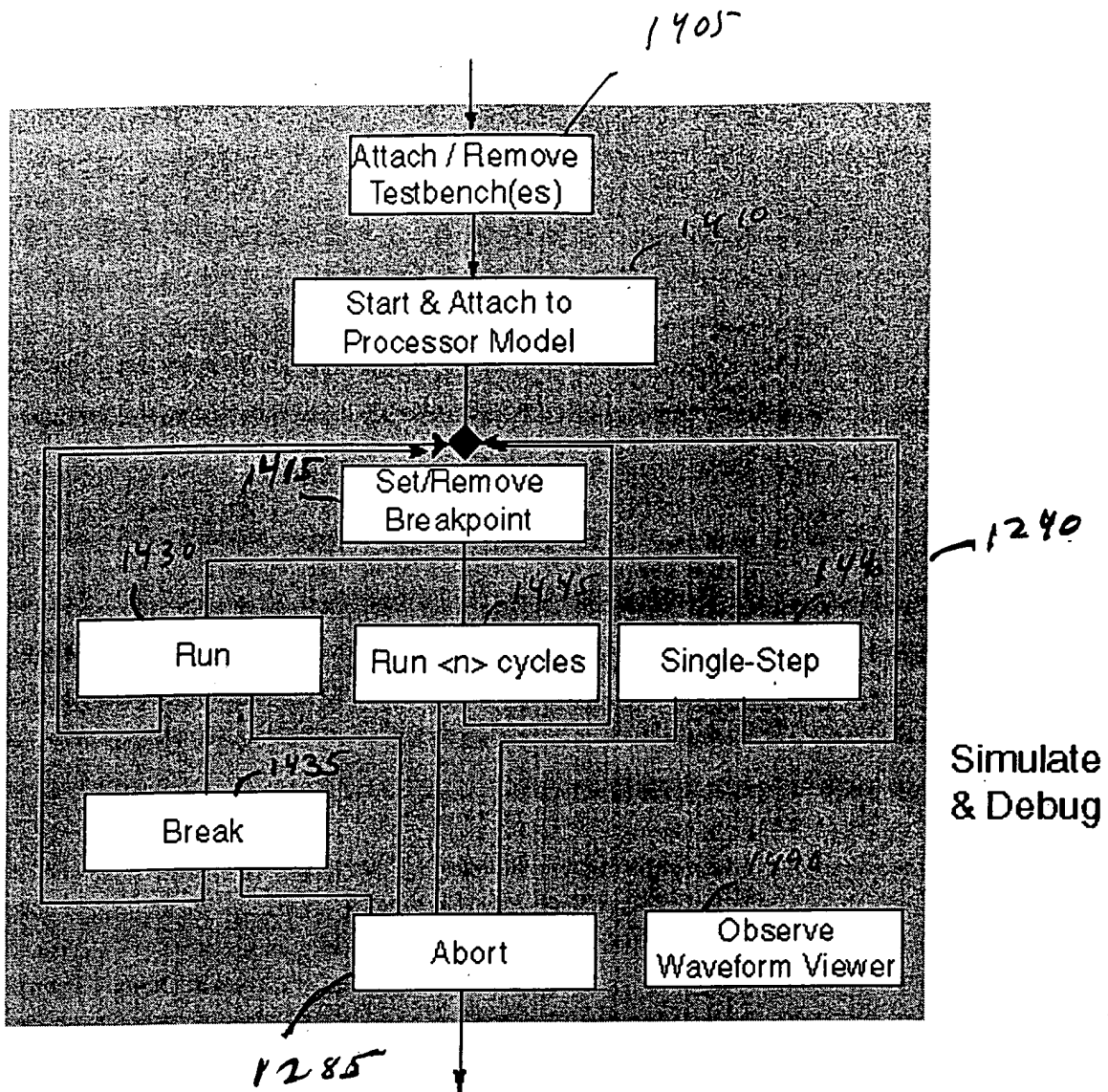
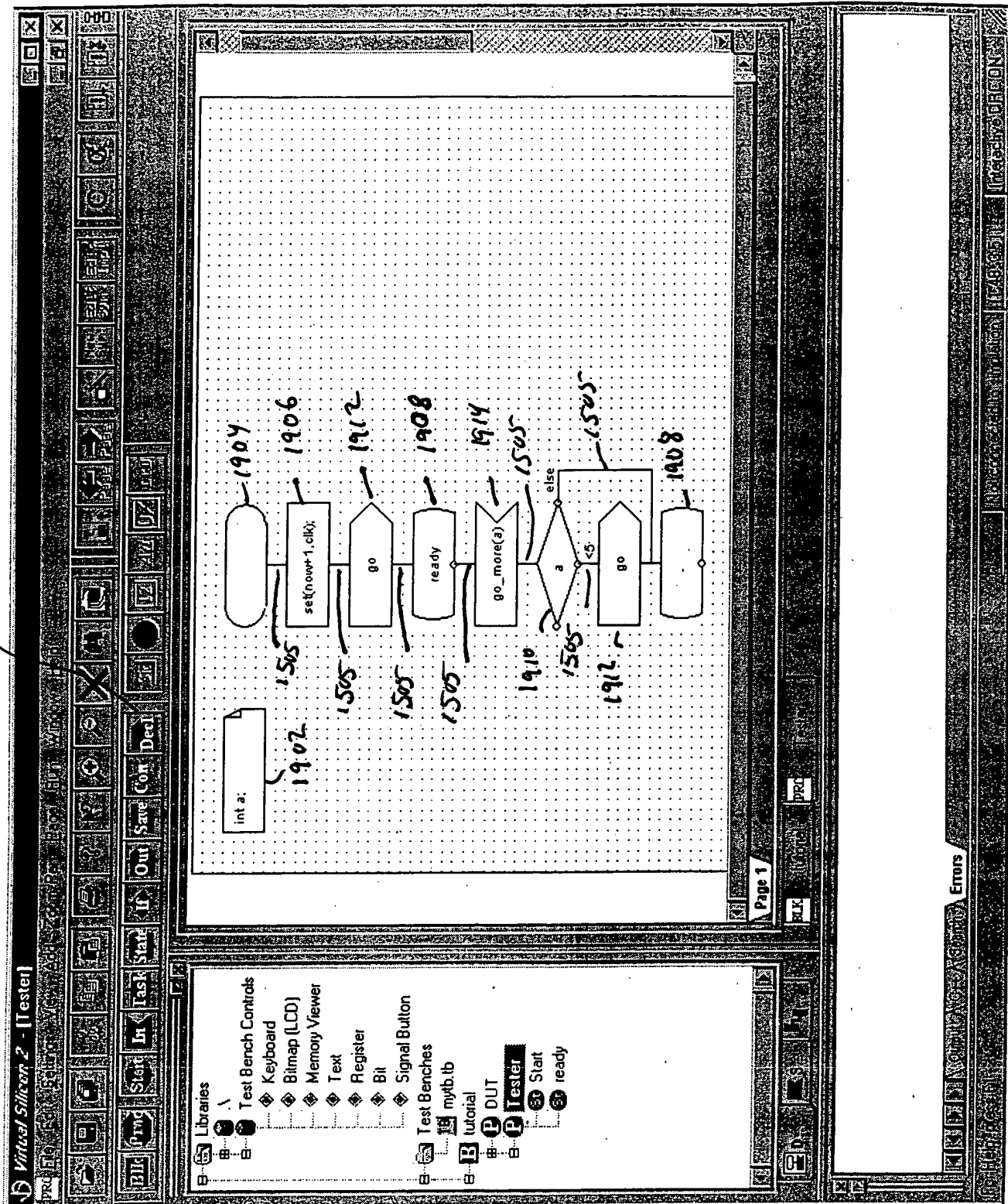


FIG. 14





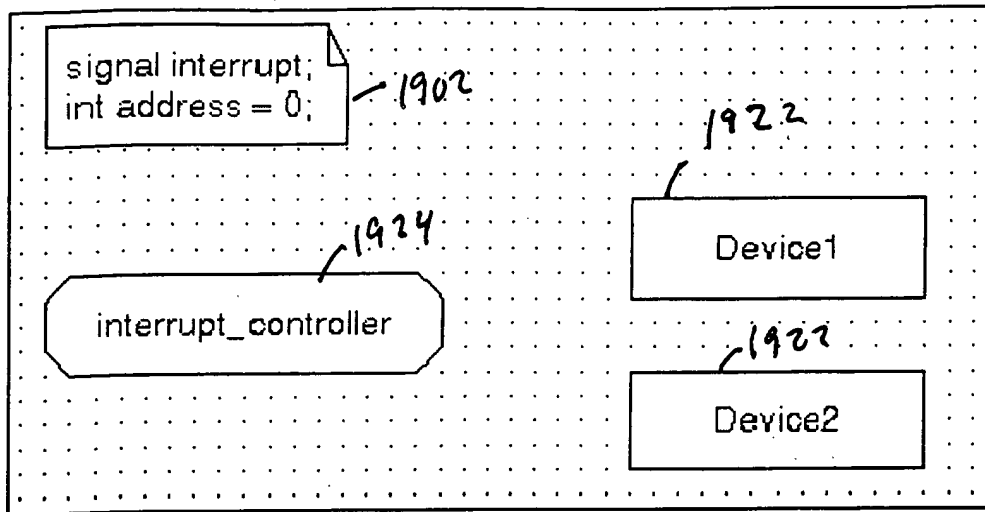


FIG. 16

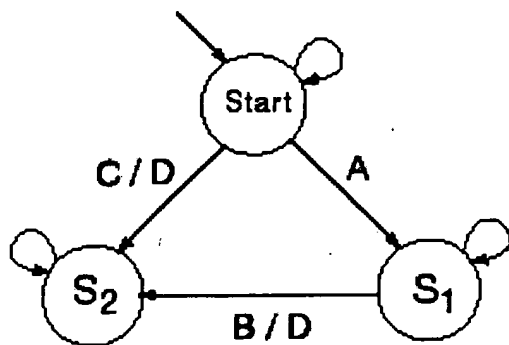


FIG. 17a)

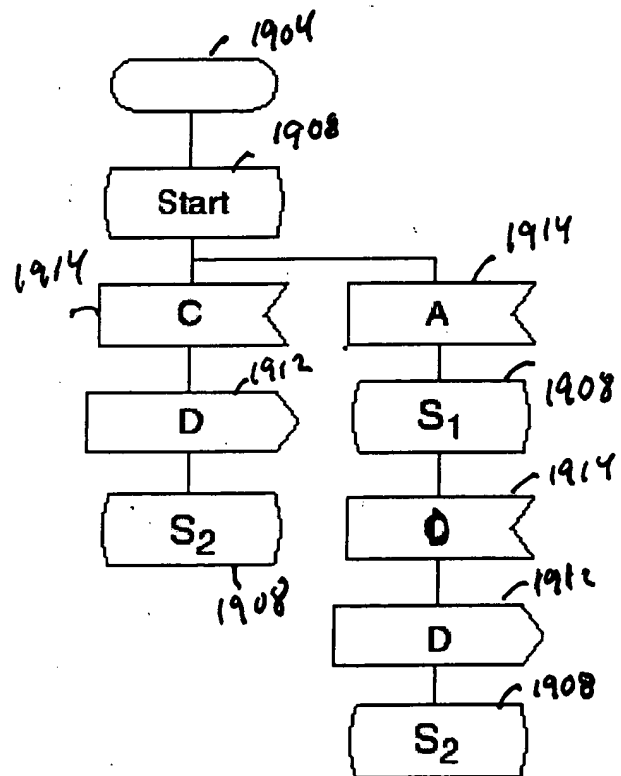
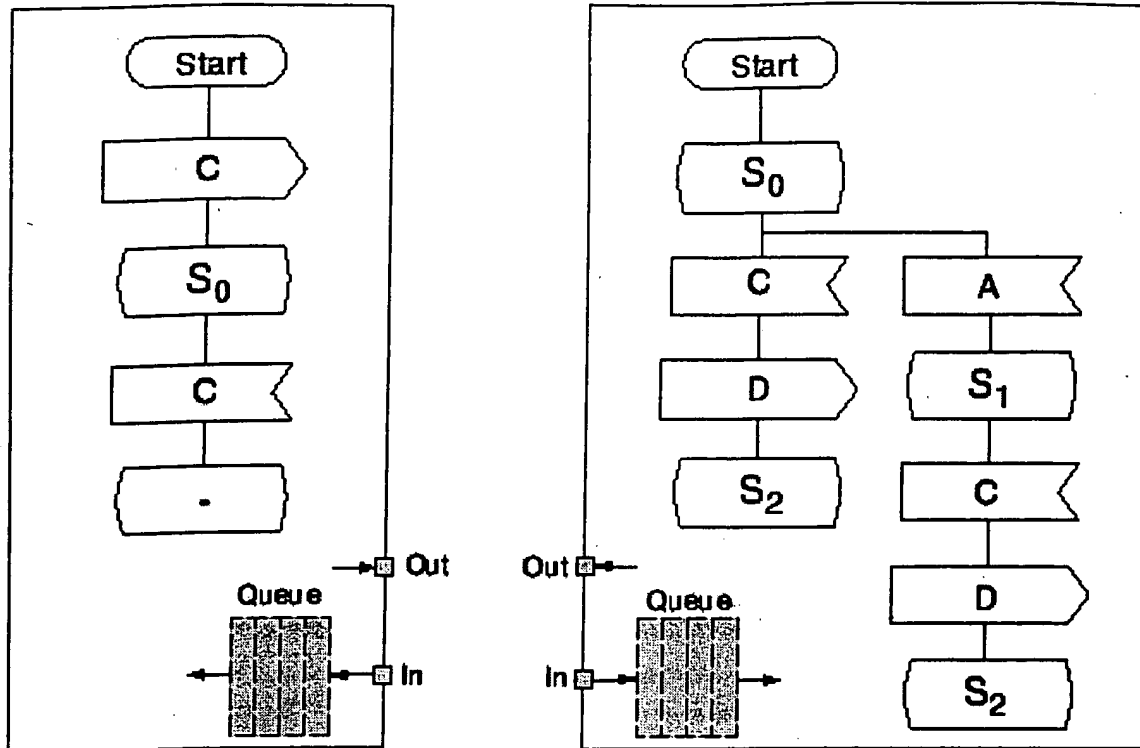


FIG. 17 (b)



FJG.18

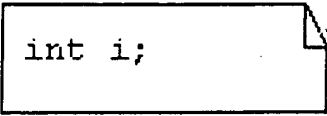
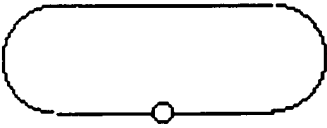
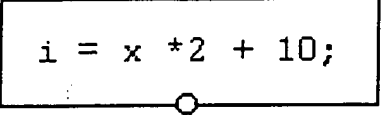
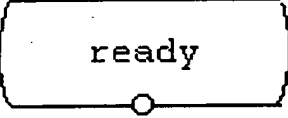
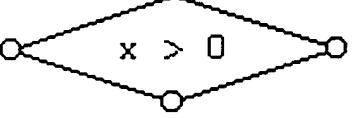
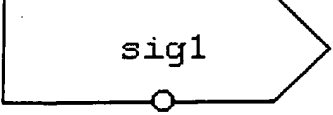
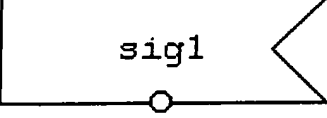
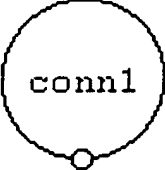
Name	Graphical symbol	Description
Declaration		defines local variables and signals.
Start		Starting point of the Finite State Machine execution at initialization time.
Task		Execution block, containing ANSI-C statements to be executed.
State		Location where FSM waits in until a triggering Signal is received.
Decision		Directs execution flow based on the result of expression evaluation inside the decision construct.
Signal-Out		Sending of a communication signal (with an optional payload).
Signal-In		Receiving of a communication signal (with an optional payload)
Connector		Allows to split designs over multiple pages, and connects the control flow between these different pages.

FIG 19A

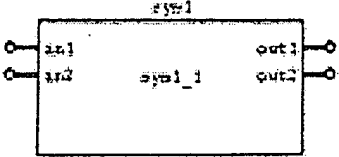
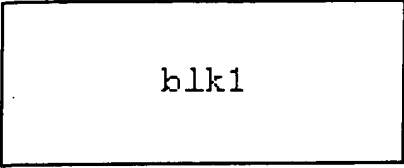
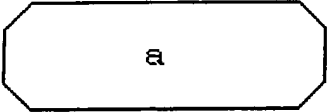
1920 Symbol		Captures design hierarchy and structure. Communication is done through pins on the outline of the symbol. Allows to re-use functional behavior by supporting multiple instances.
1922 Blocks		Captures design hierarchy and structure. Communication is done through signals declared at higher scopes. Communication is done by signal name matching (rather than by pin connection). A block can contain multiple processes.
1924 Process		Acts as leaf node in the design hierarchy, and captures a single FSM. By definition, all processes are concurrent at all times.

FIG. 19B

```

// External interface
extern_signal WR(unsigned int,unsigned int, unsigned int);
extern_signal RD(unsigned int,unsigned int);
extern_signal Write_Ack;
extern_signal Read_Data(unsigned int);
extern_signal CNTINTR(unsigned int);
// Local variables
signal start_clk;
clock clk;
bool clock_started;
unsigned int LIMIT; //write register
VS_int COUNT;
//temp vars
unsigned int data,width, addr;

```

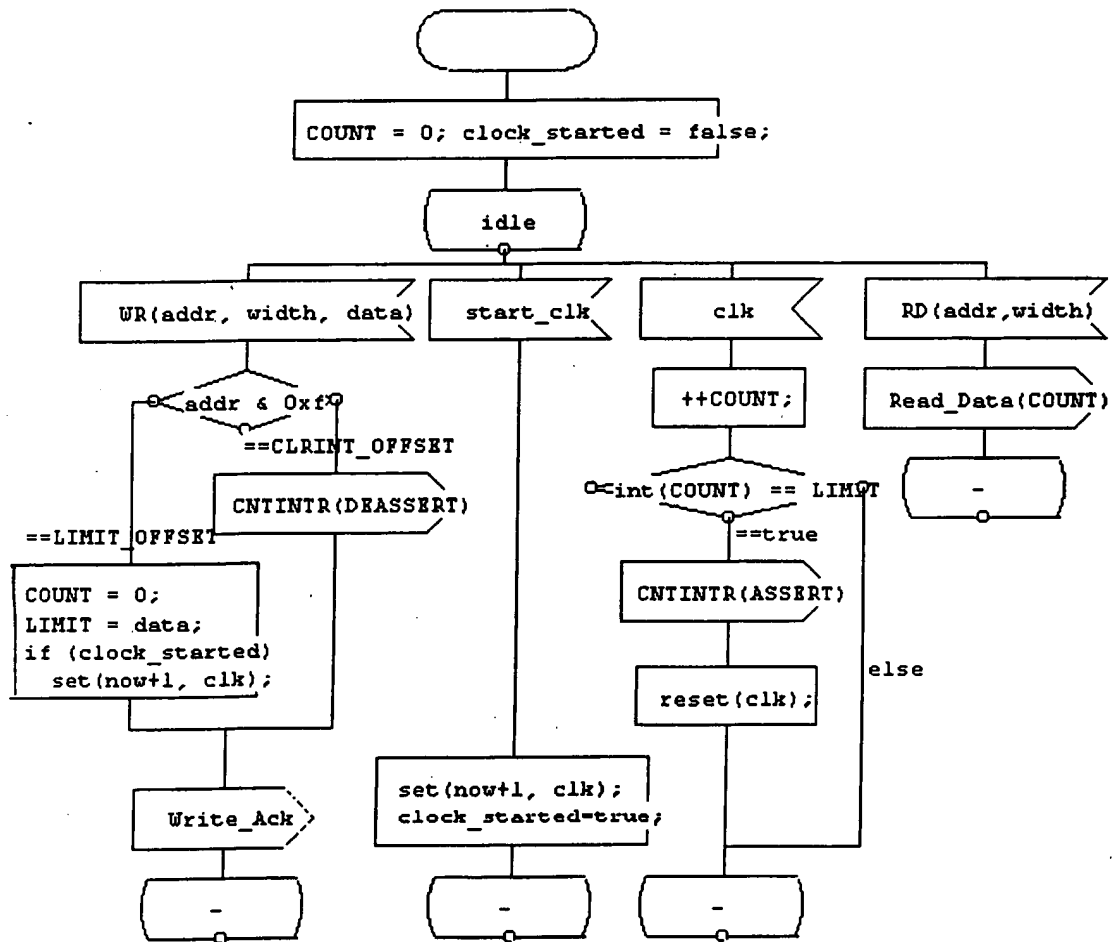


FIG.20

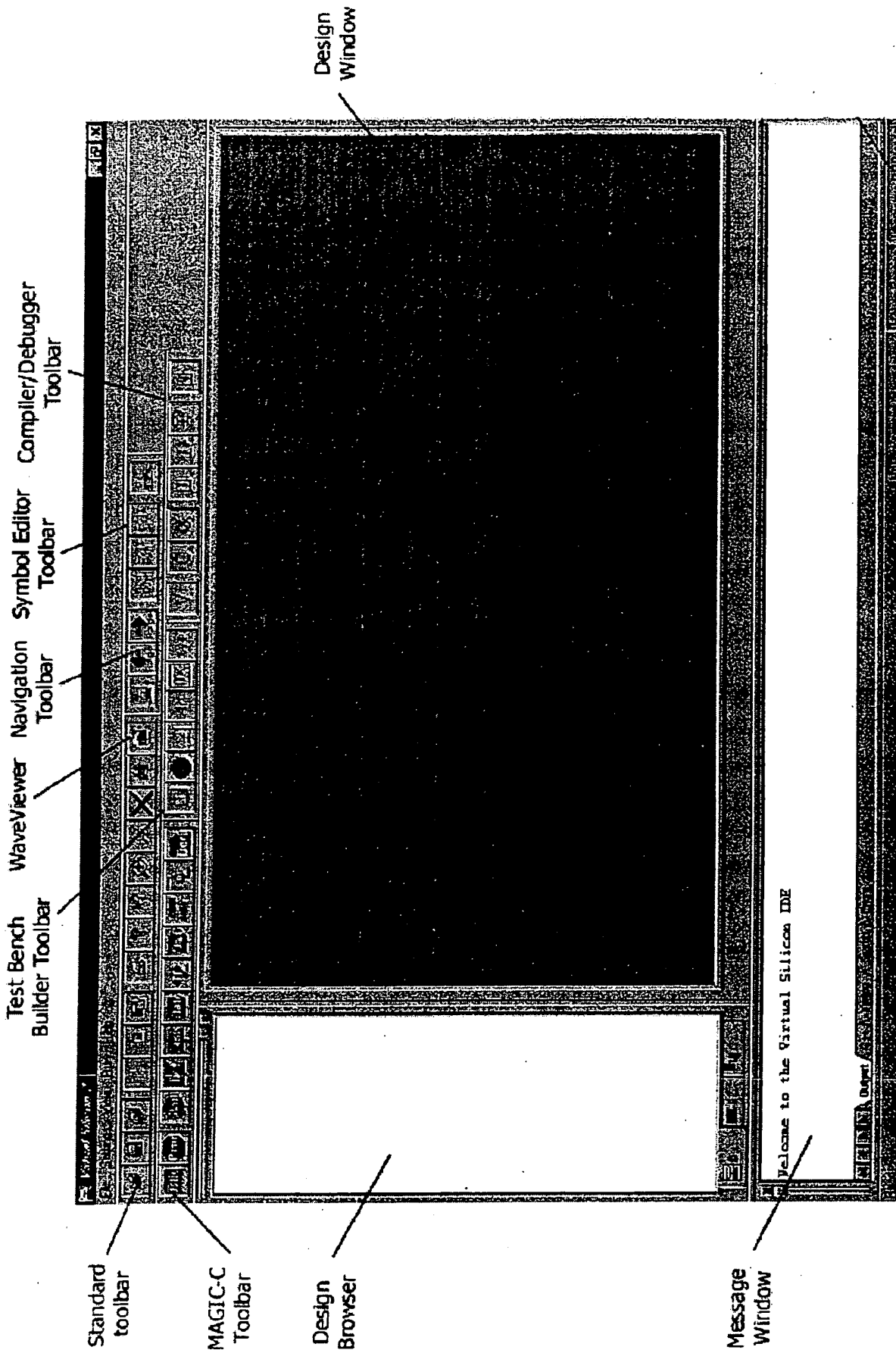


FIG. 21





FIG. 22

Standard Toolbar

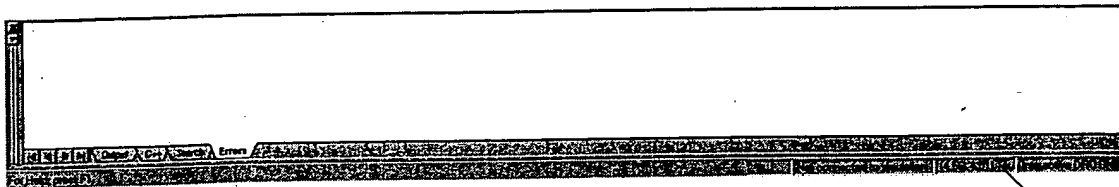
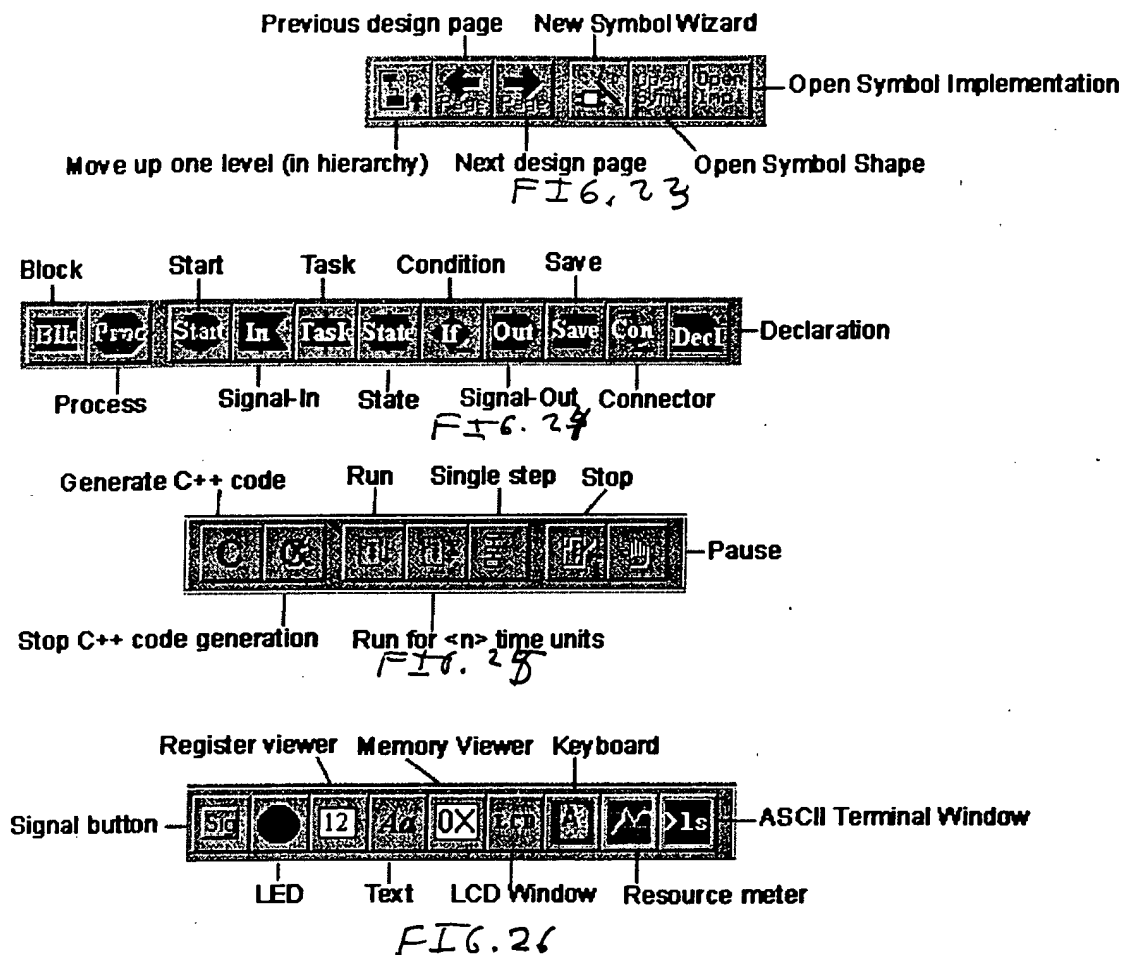


FIG. 23

Status Bar

Message Window, Showing Different Message Tabs, and the Status Bar



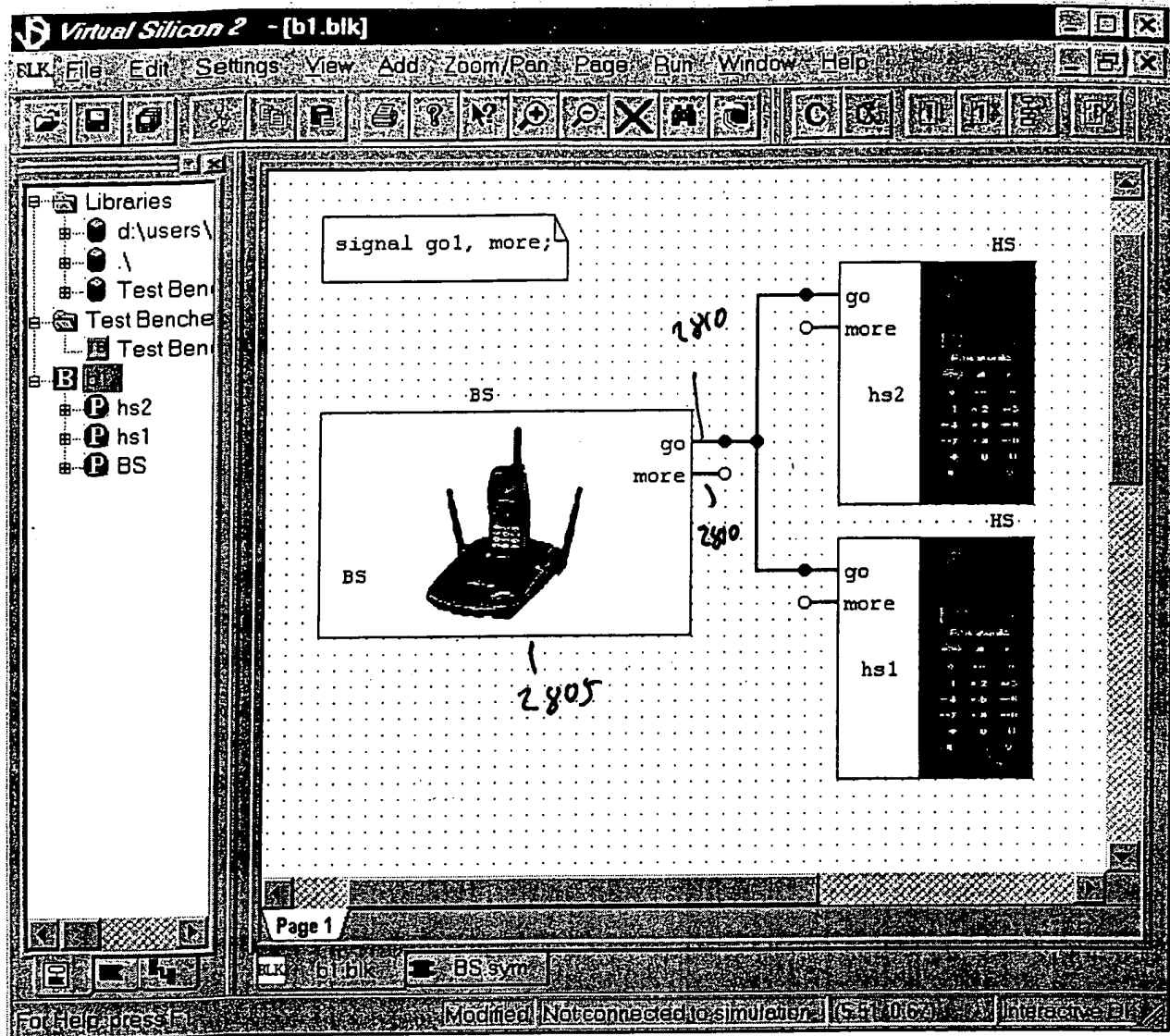


FIG. 28

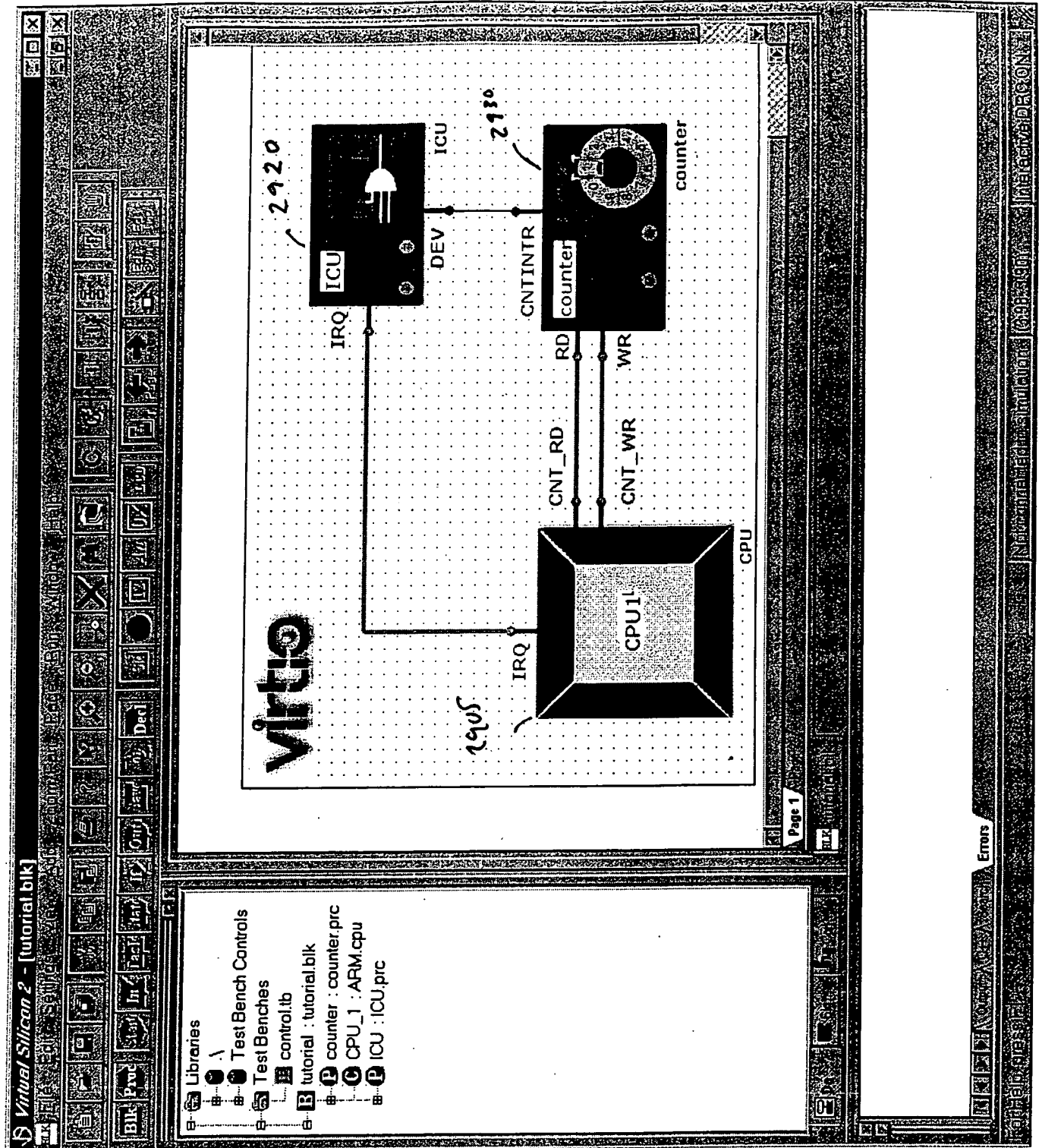


FIG. 29

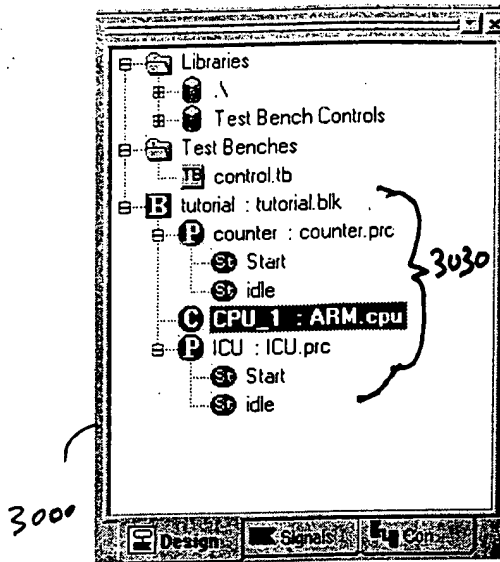


FIG. 30

3020

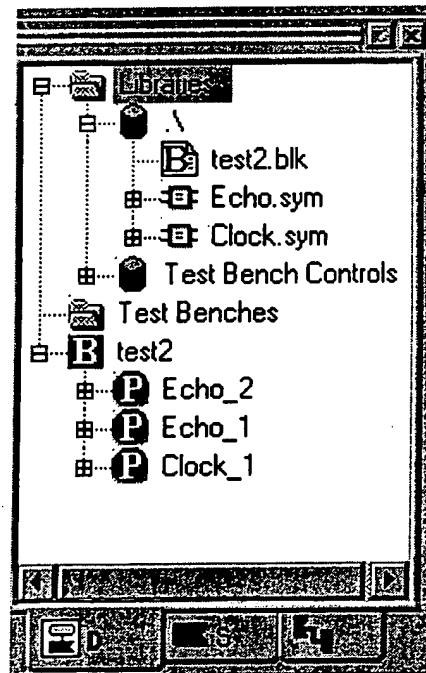
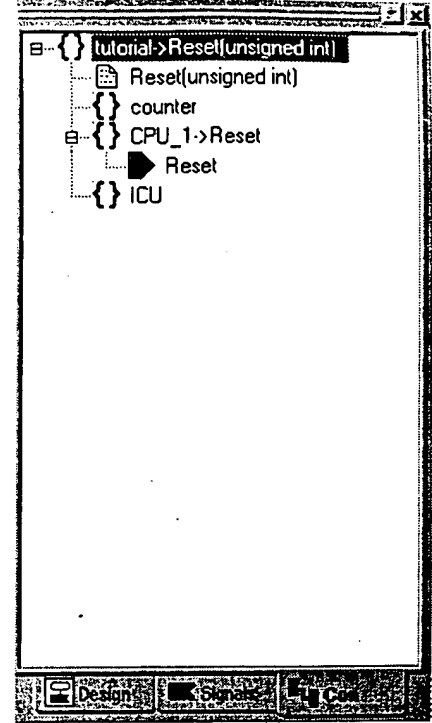
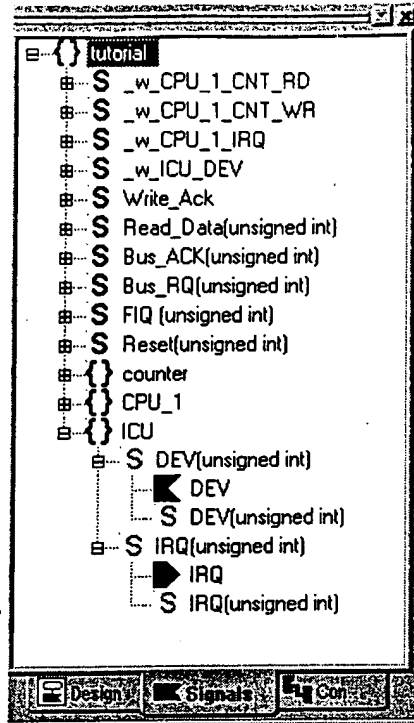


FIG. 31

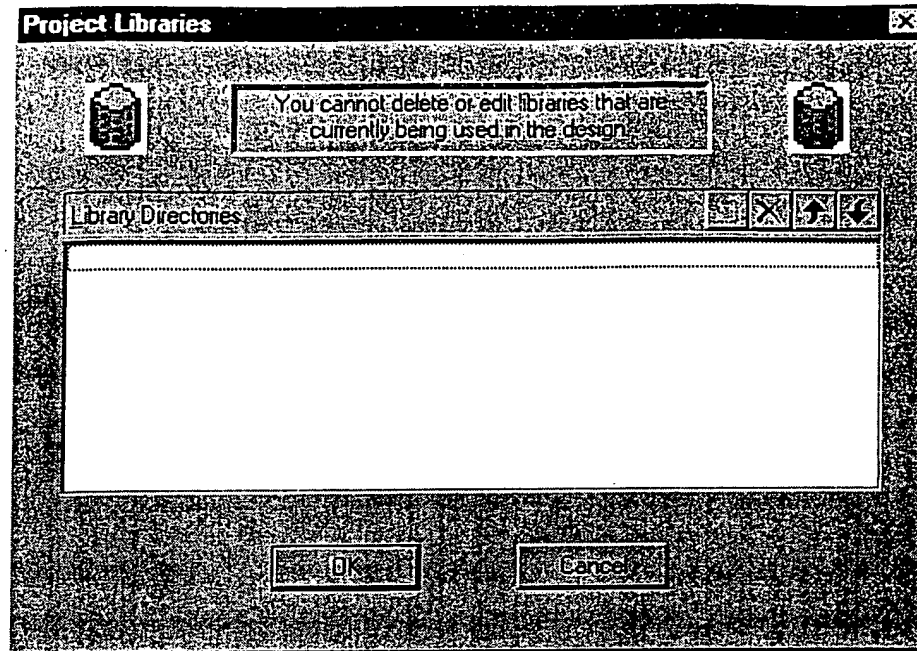
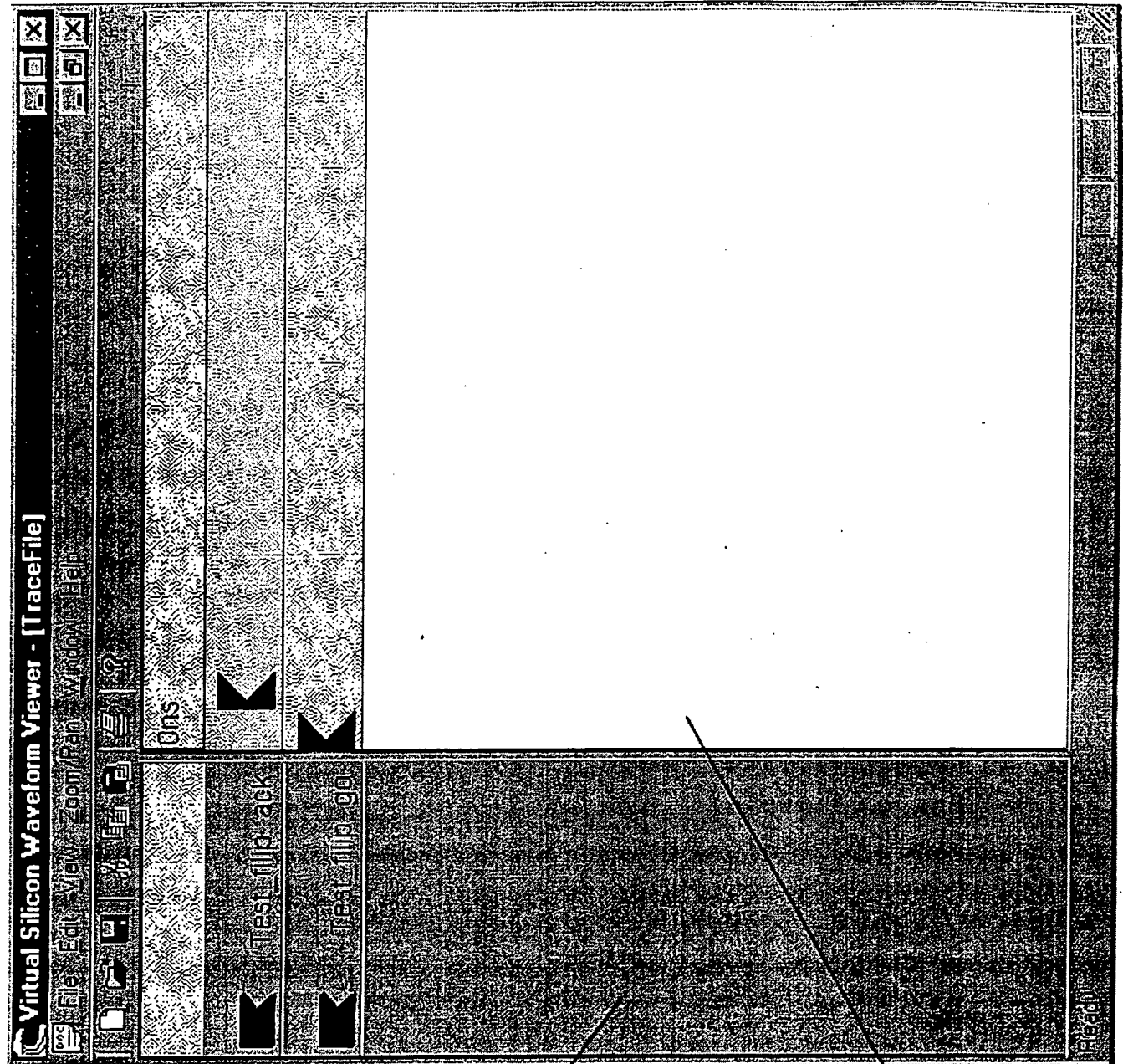


FIG. 32



Name Display  
Window

Waveform  
Display

FIG. 33A



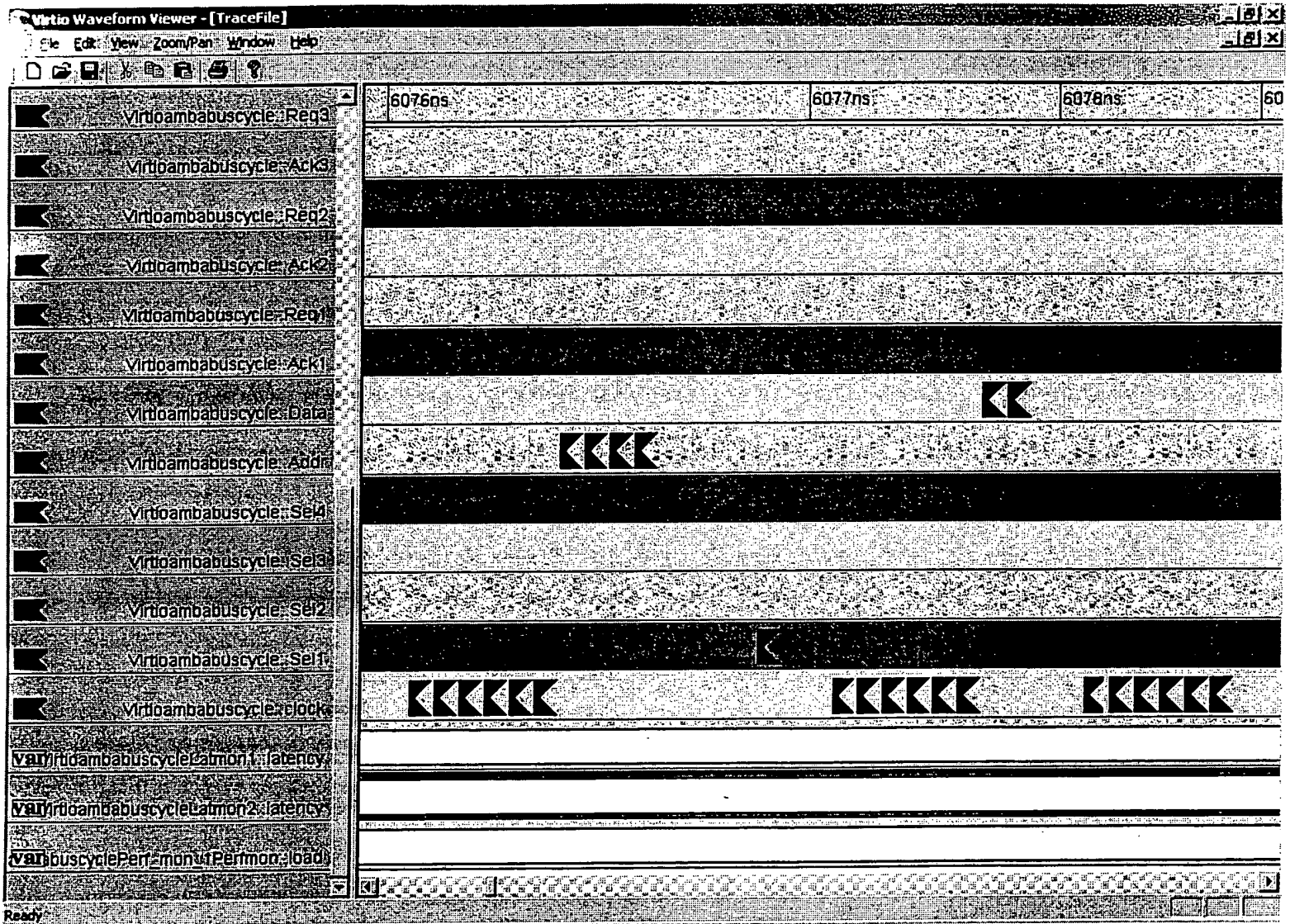


FIG. 33b

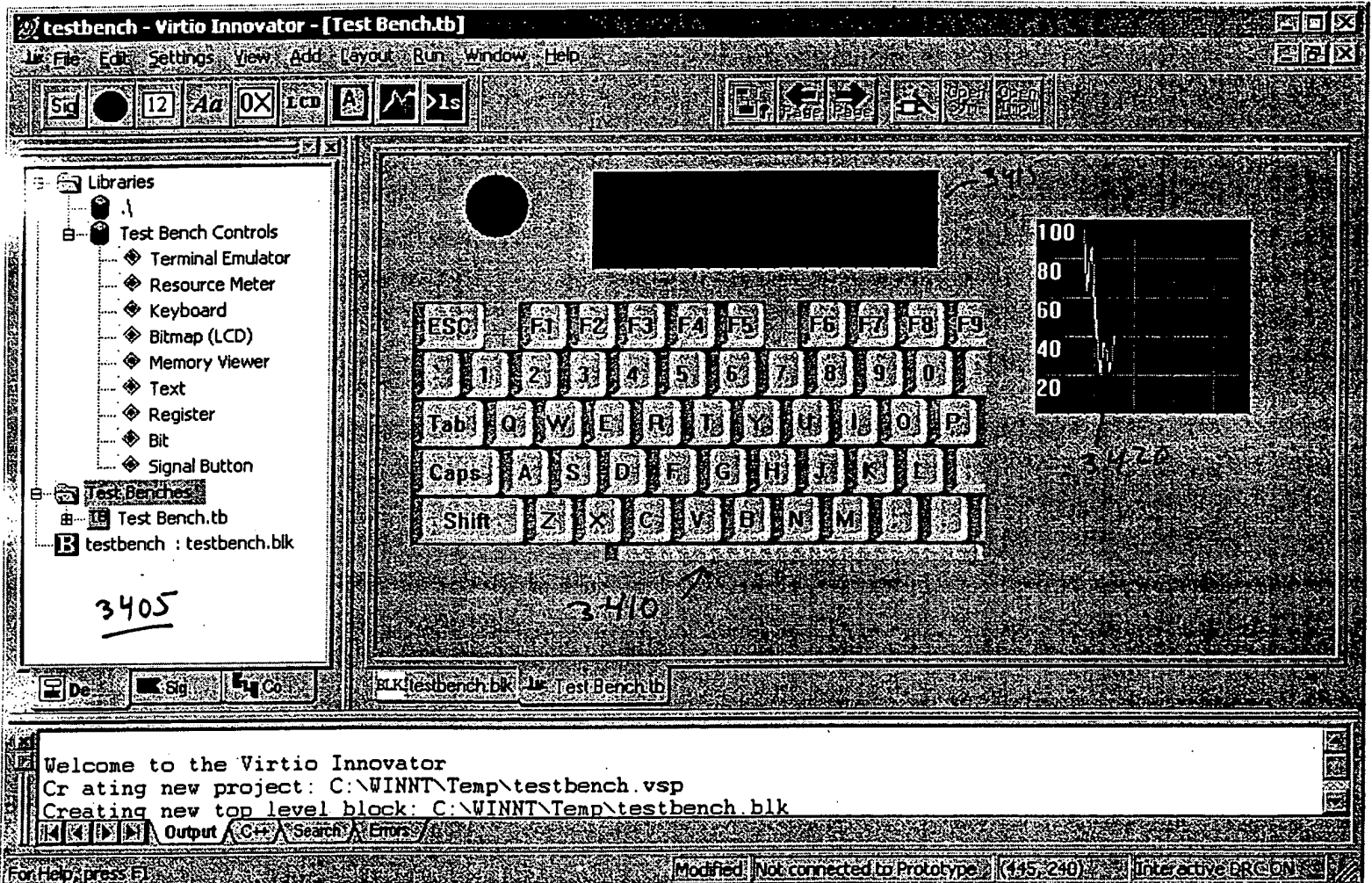


FIG. 34A

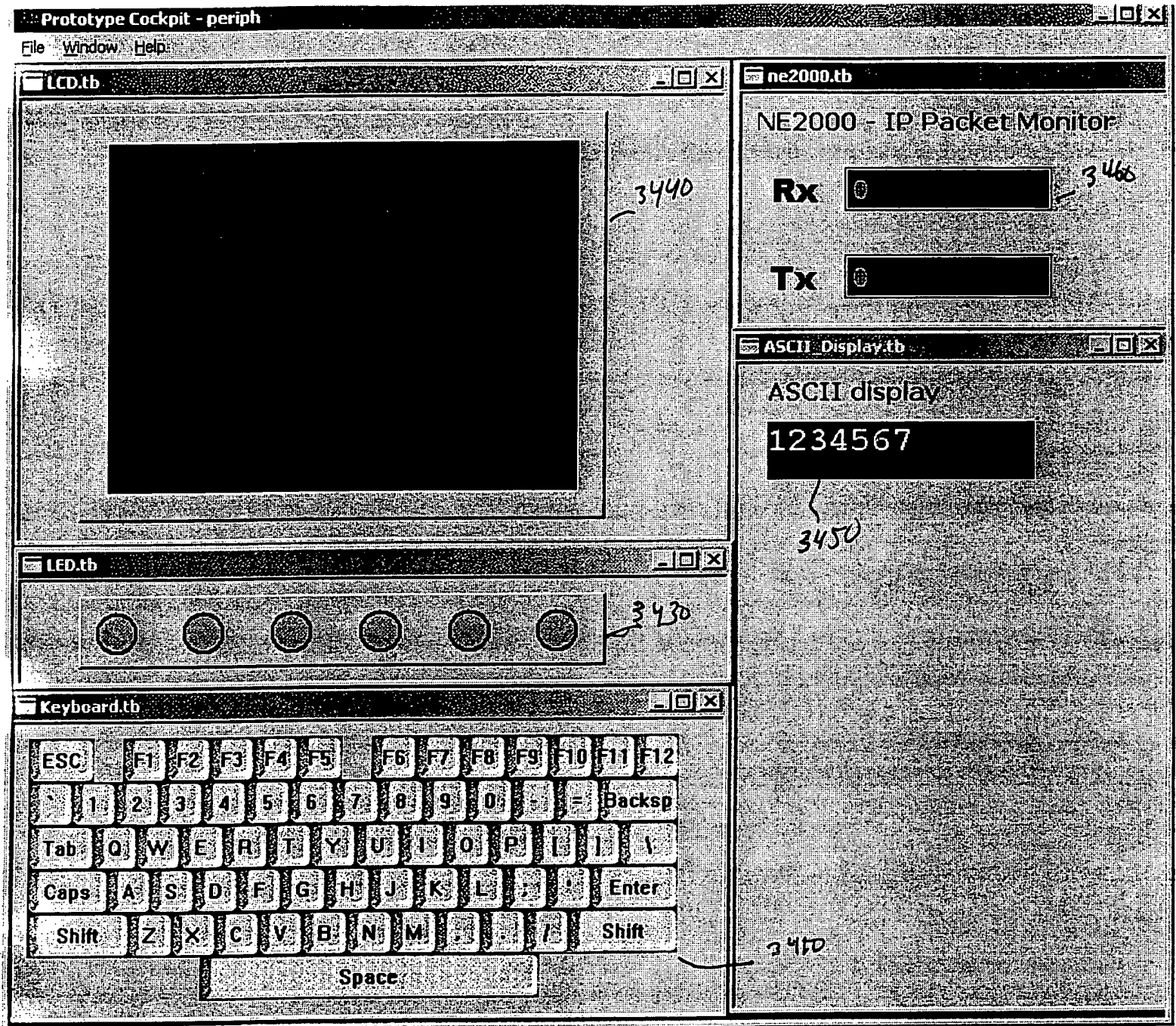
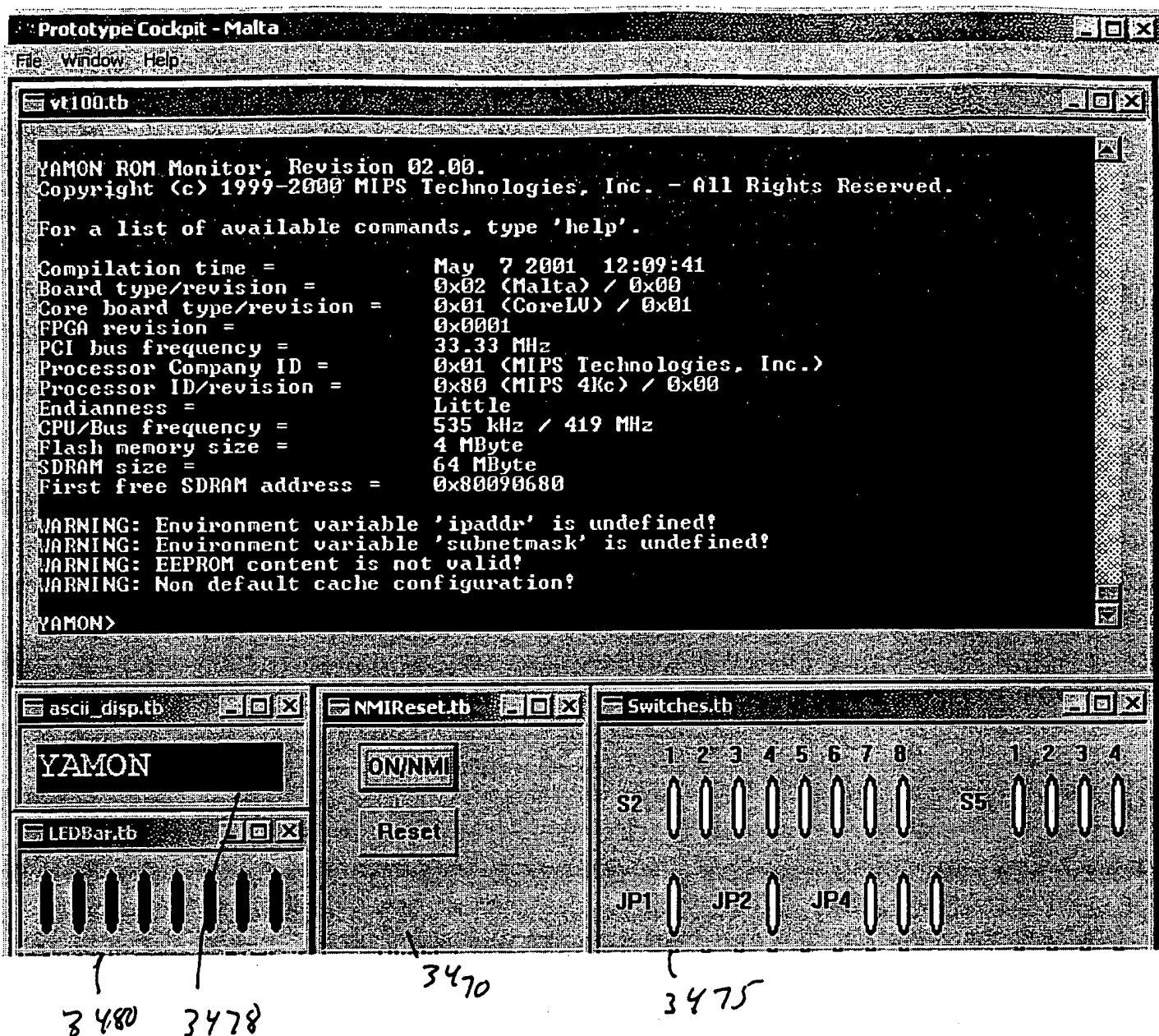


FIG 34B



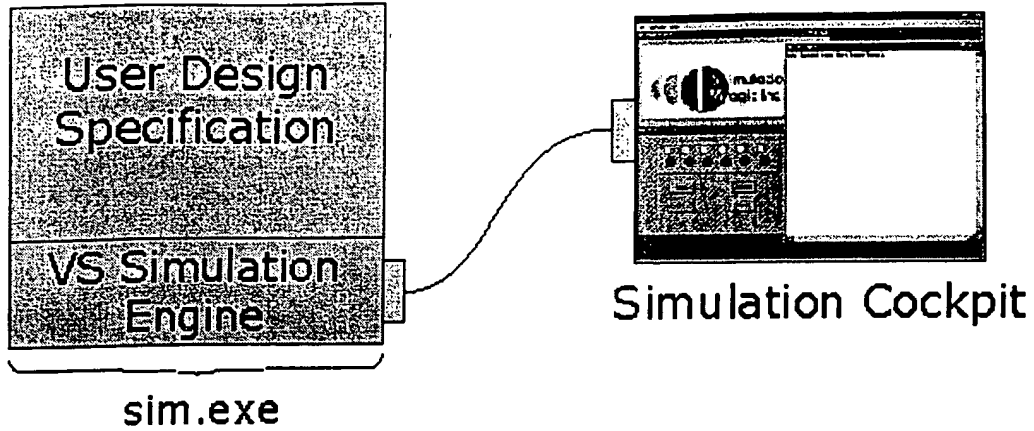
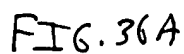
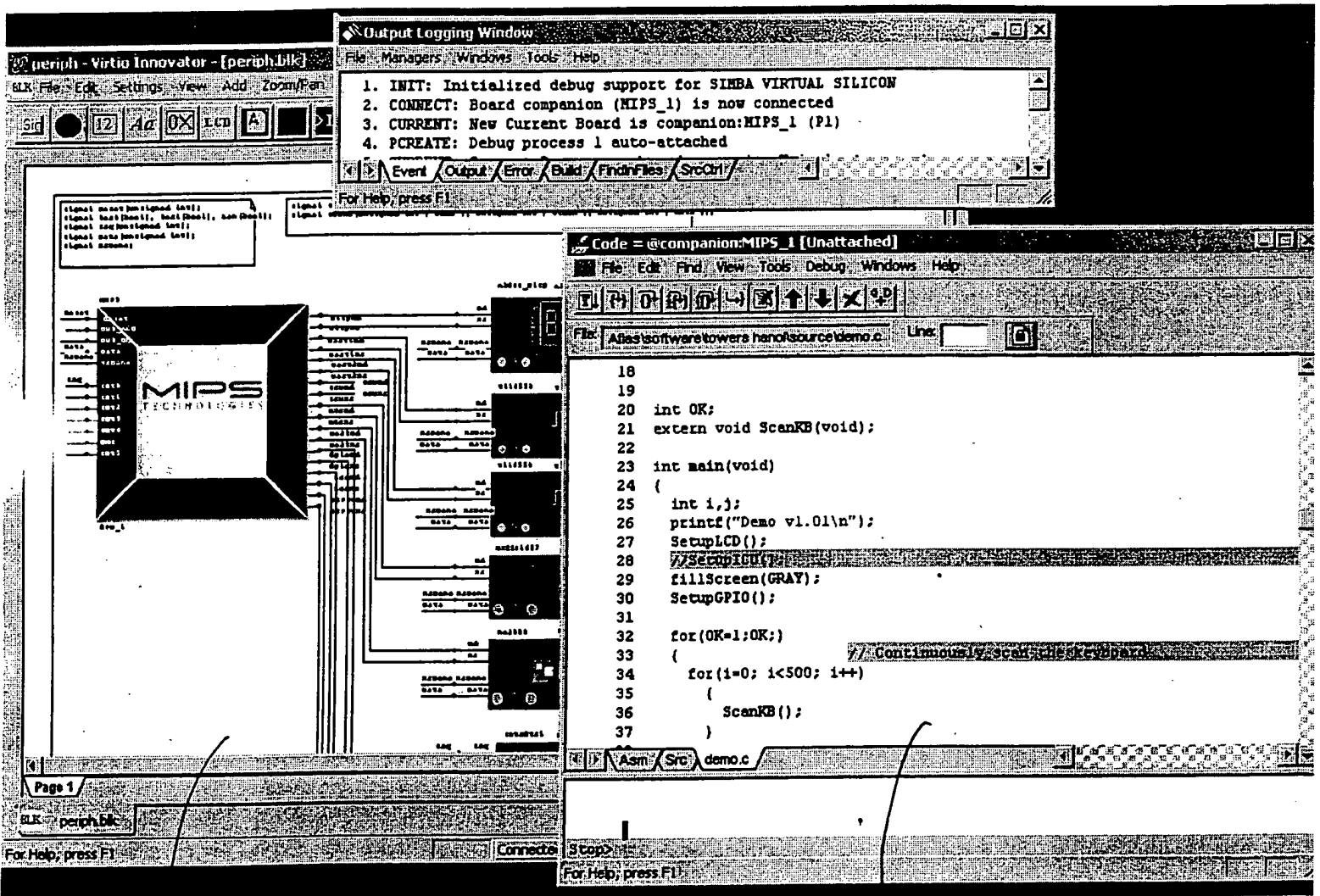


FIG. 35







3620

FIG. 36B

3685



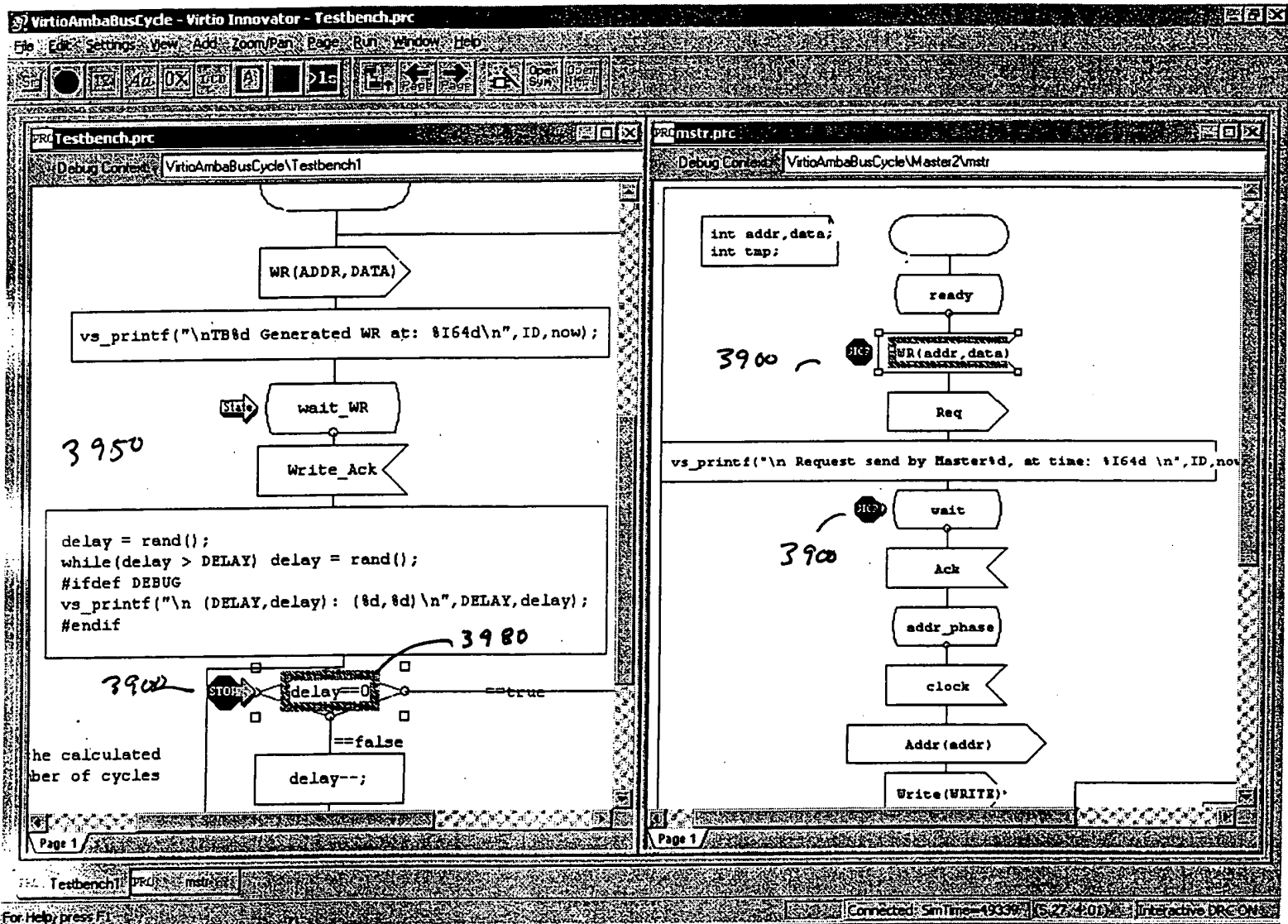


FIG. 36C

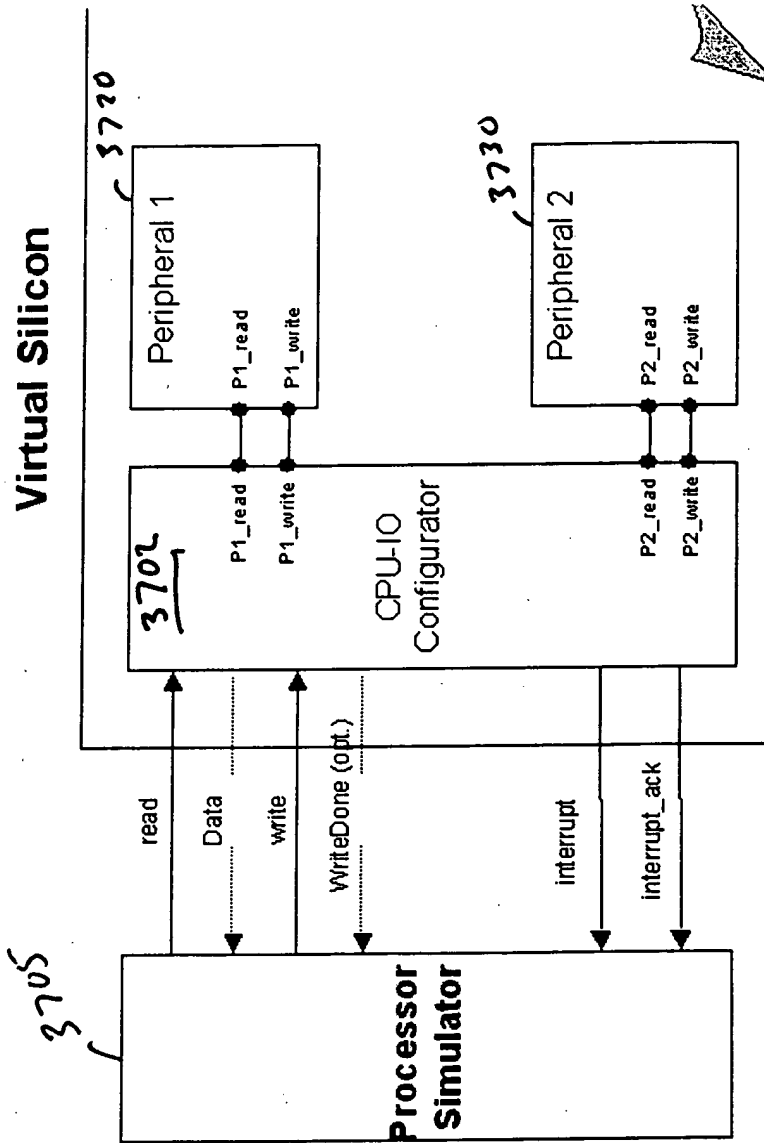


FIG. 37

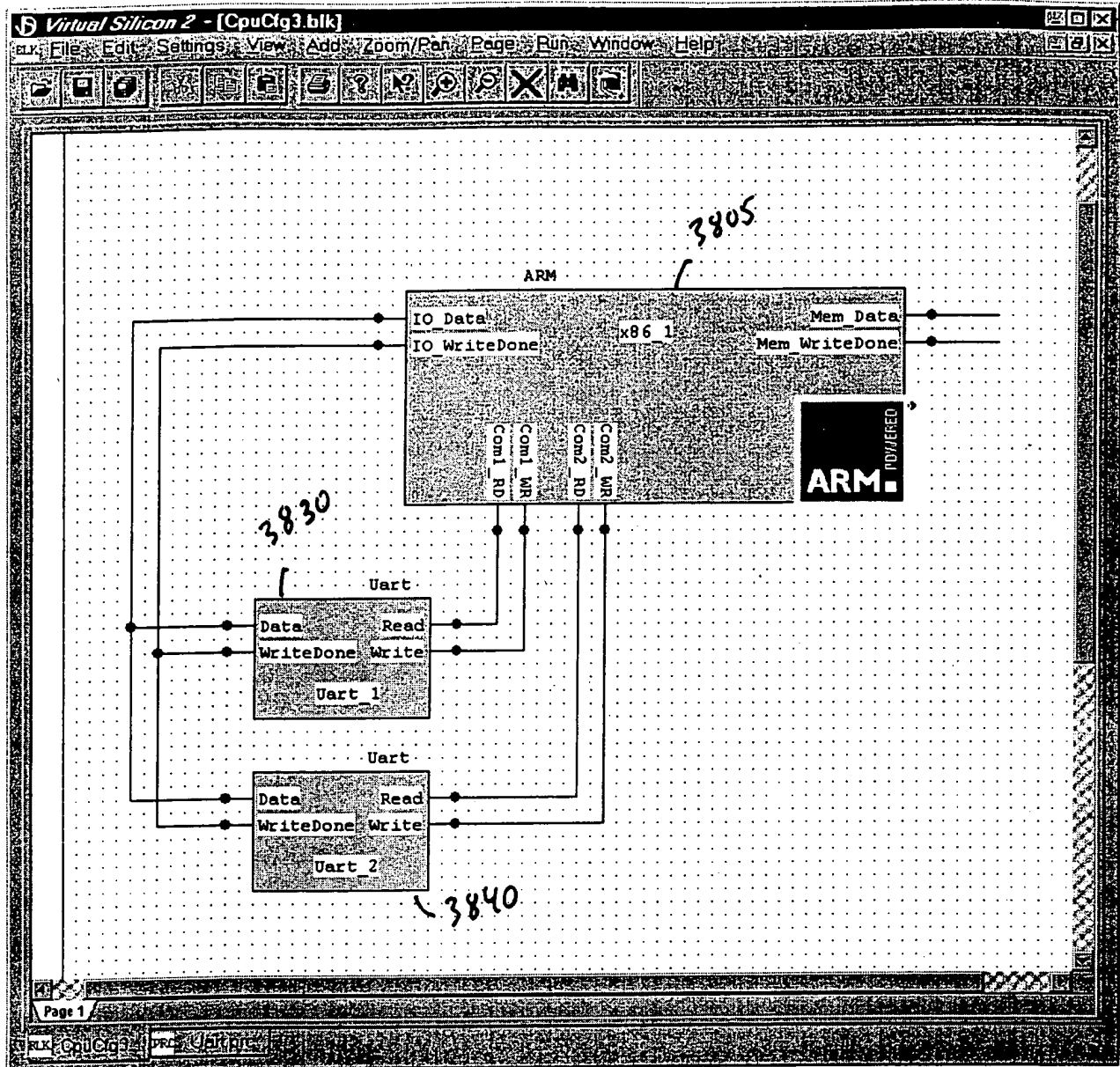


FIG. 38

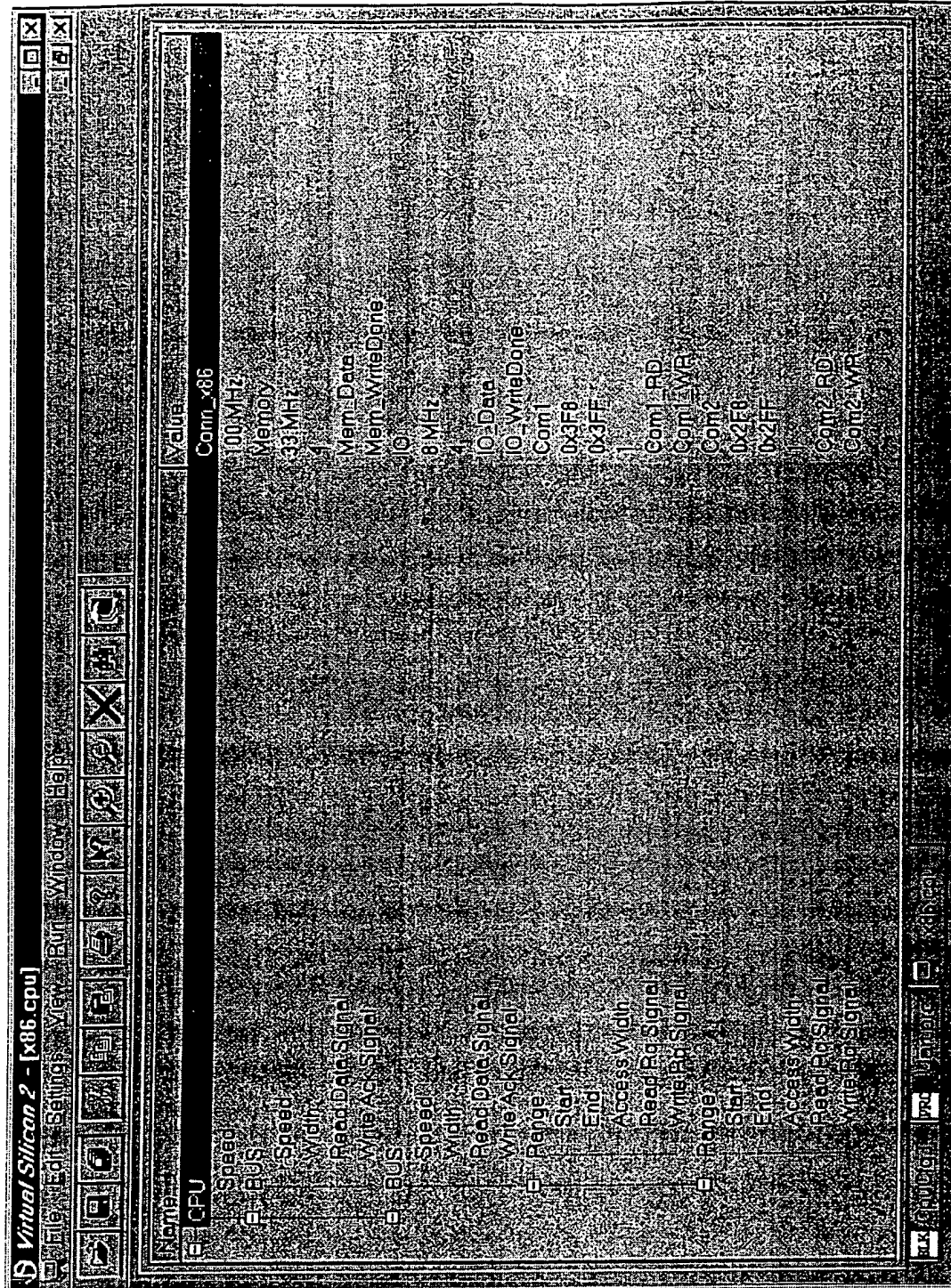


FIG. 39

Name	Value
<input checked="" type="checkbox"/> CPU	ArmCPU
Speed	100 MHz
<input type="checkbox"/> Events: CPU > Simulation	
RESET Signal	Reset
BUS ACK Signal	Bus ACK
<input type="checkbox"/> Events: Simulation > CPU	
BUS RD	Bus RD
<input type="checkbox"/> Interrupt Support	Yes
FIQ Signal	FIQ
IRQ Signal	IRQ
<input checked="" type="checkbox"/> BUS	Memory
Speed	100 MHz
Width	32
Read Data Signal	Read Data
<input type="checkbox"/> Write Timing	Variable
Write Ack Signal	Write Ack
<input type="checkbox"/> Range	Counter
Type	Slave
Start	CNT_START_ADDR
End	CNT_END_ADDR
Access Width	4
Read Rd Signal	CNT_RD
Write Rq Signal	CNT_WR

FIG. 40

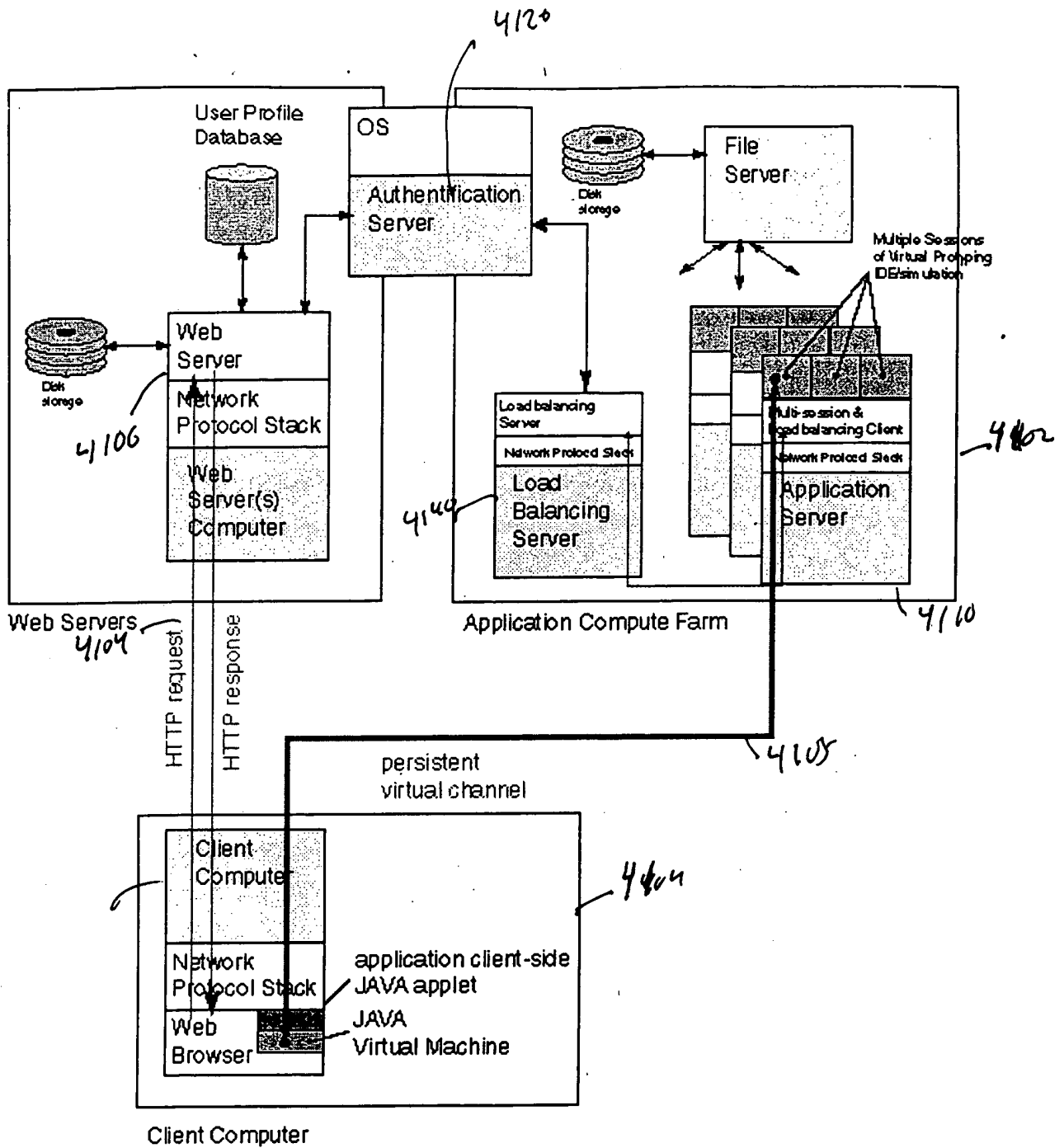
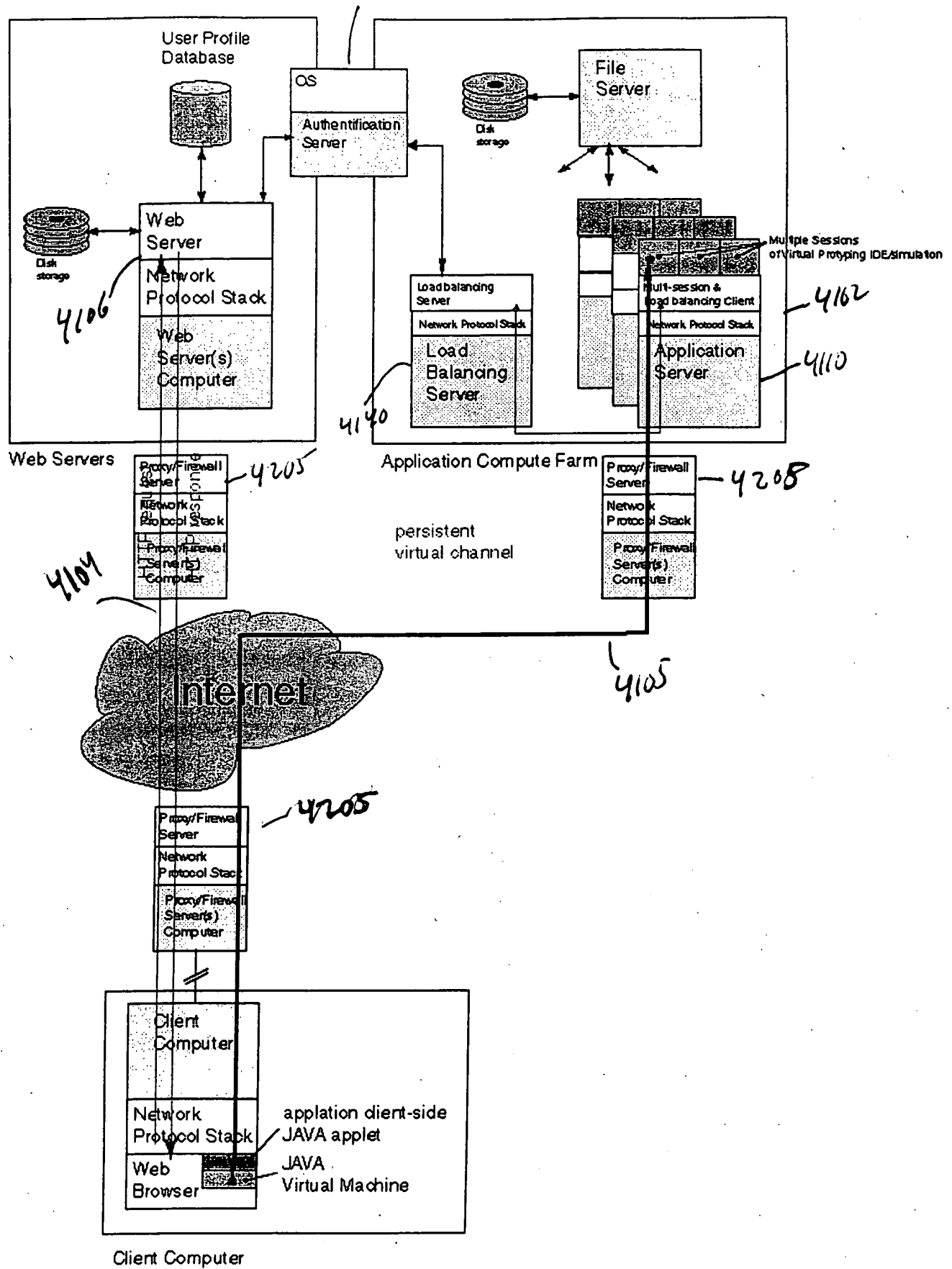


FIG. 41



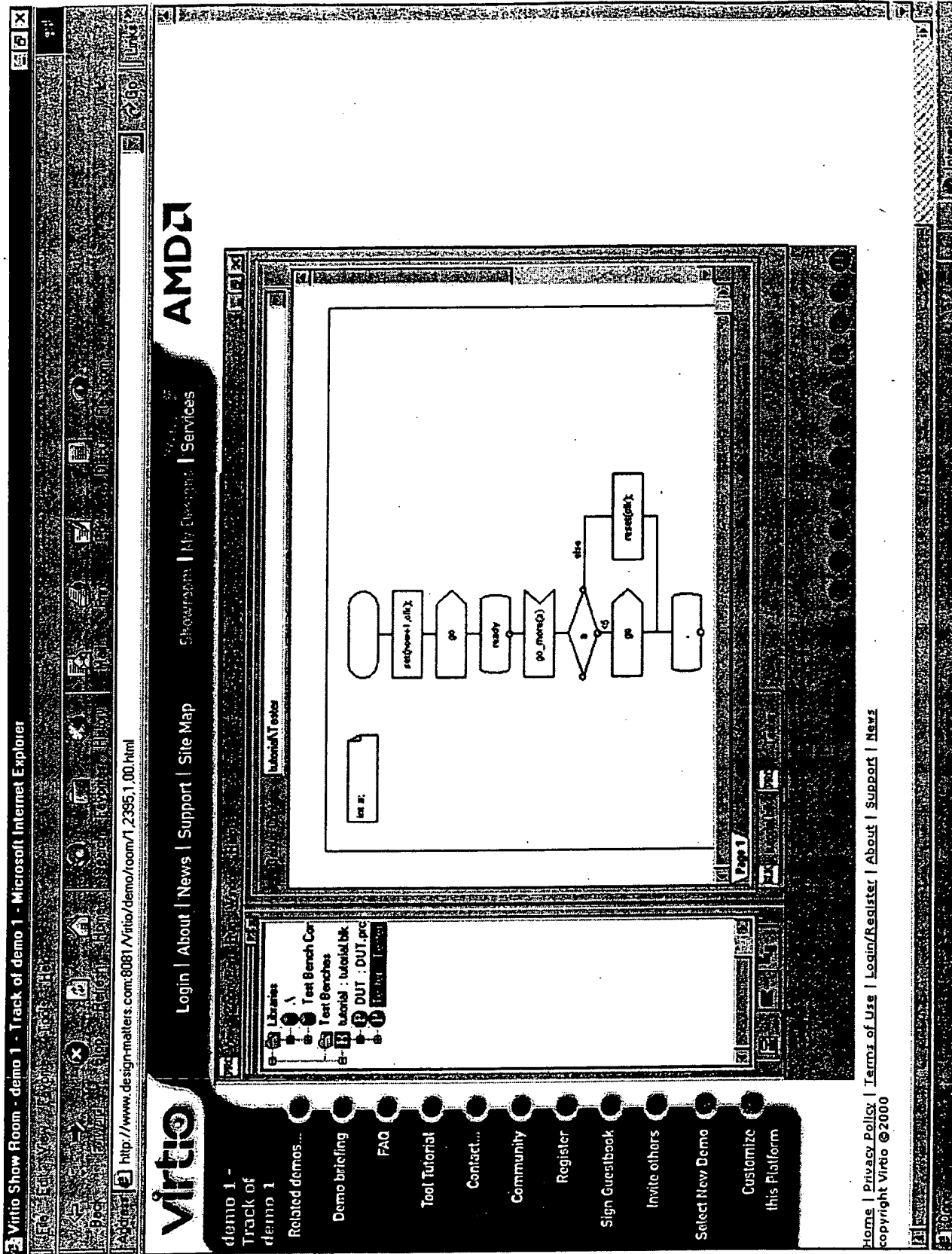


FIG-43



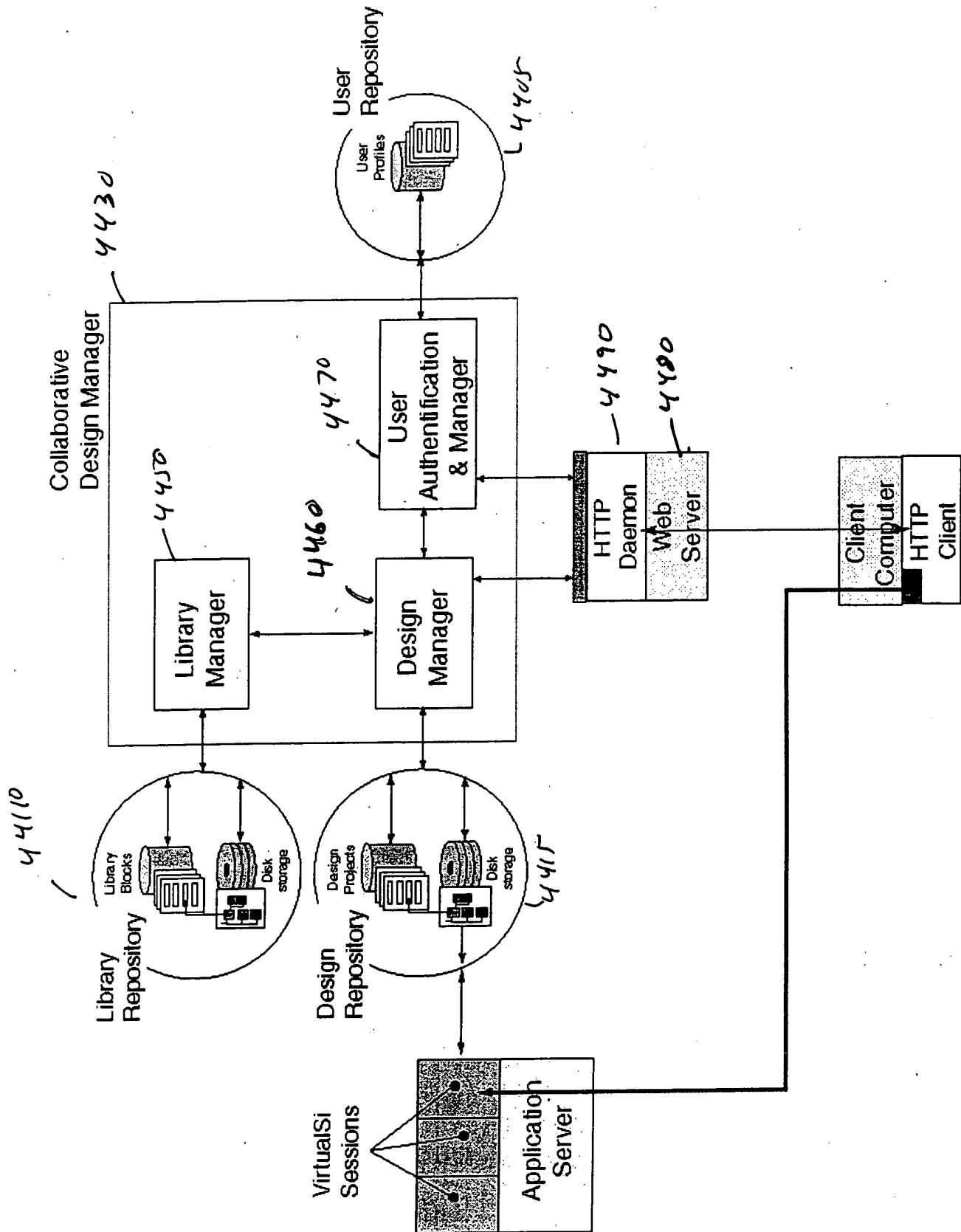




FIG-44

 Clock_1	Scope name.
 clk(int)	Signal name and declaration.







 t	Timer or clock name and declaration.
 clk	Local name of a signal coming from the upper scope (inherited).
 myClk	Timer or clock is being set.
	Signal is being sent.
	Signal is being received.
	Signal is being saved.

FIG. 45

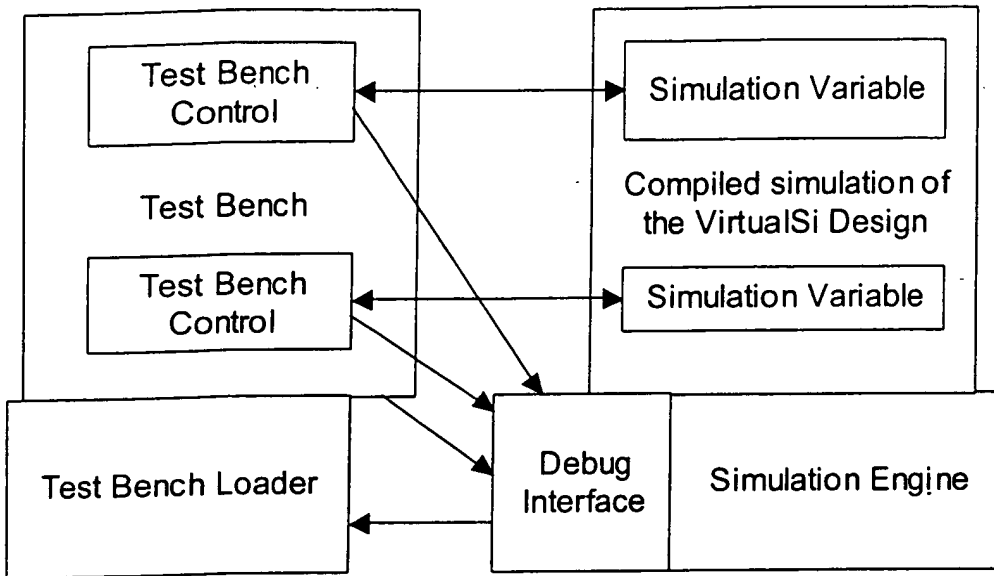


FIG. 46

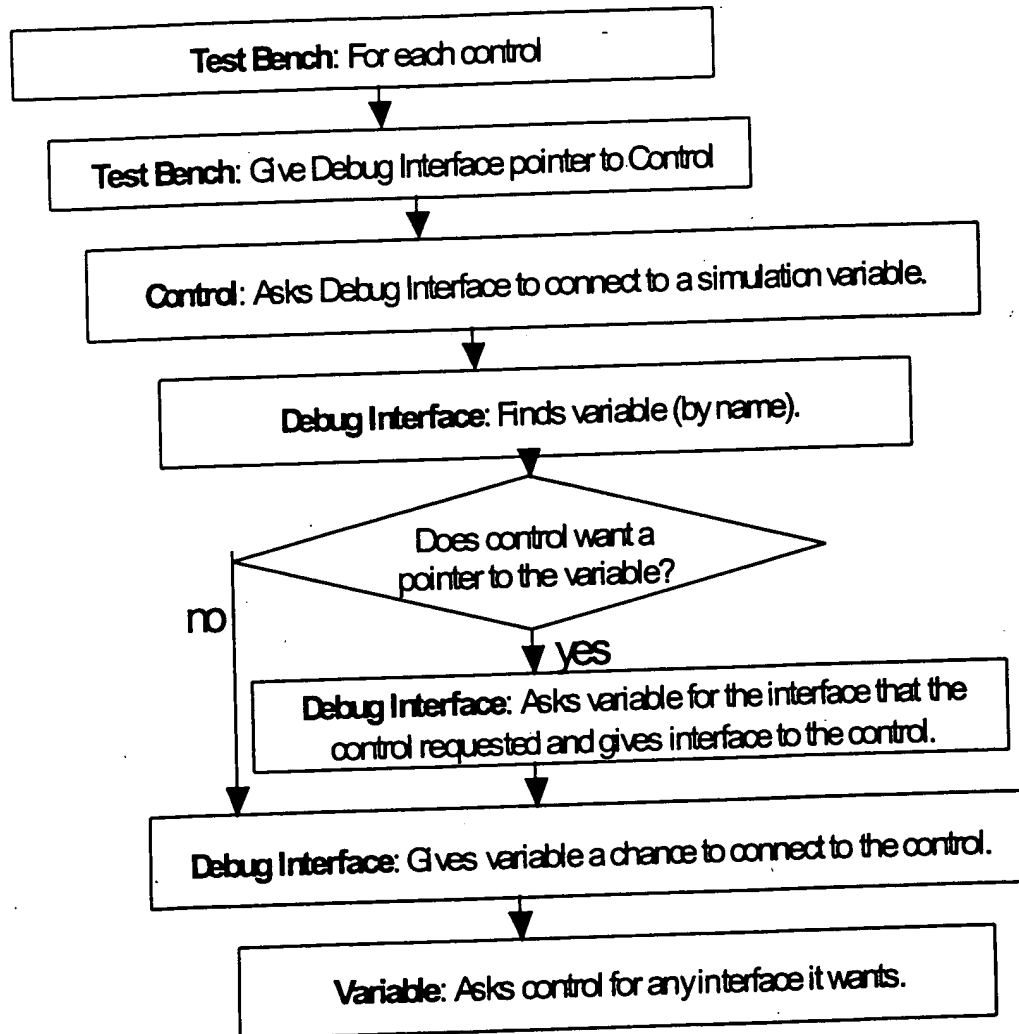


FIG. 47

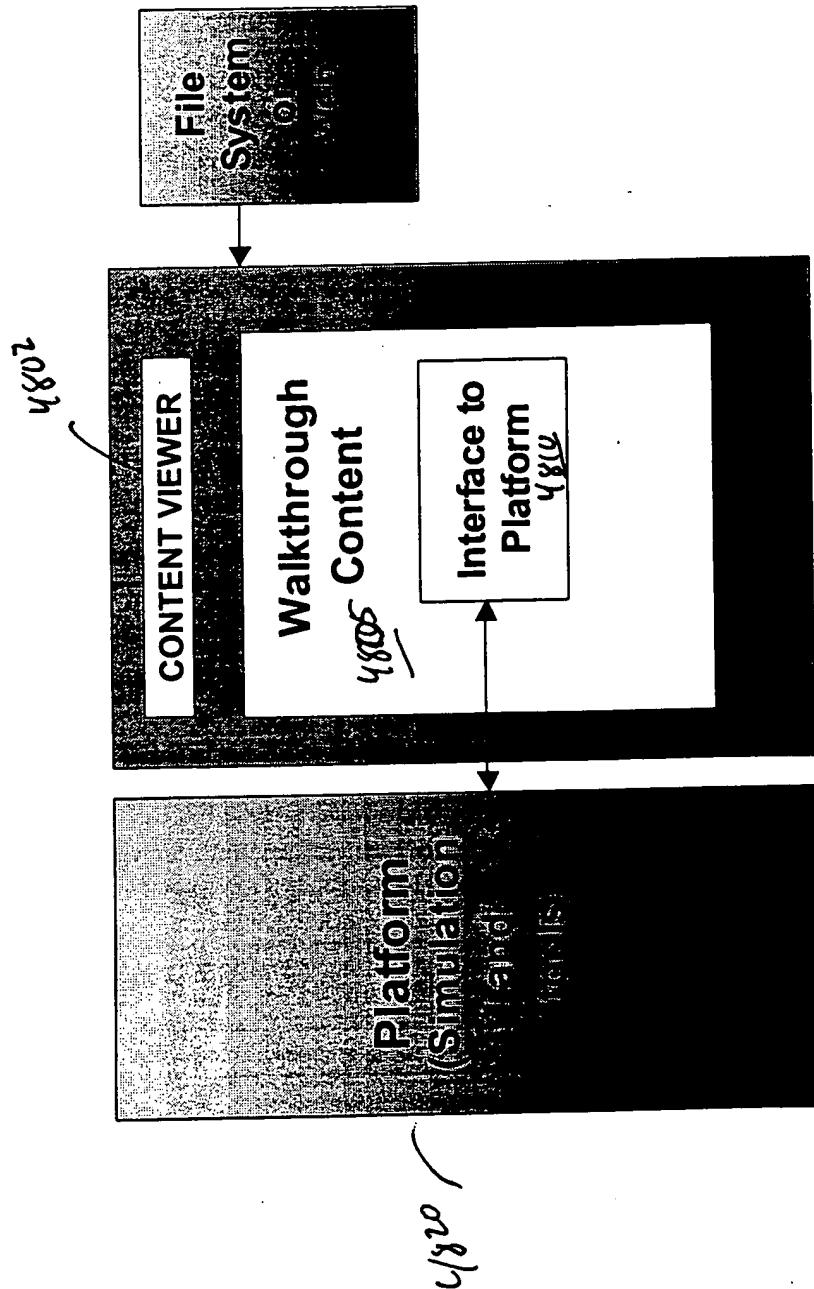


FIG. 48

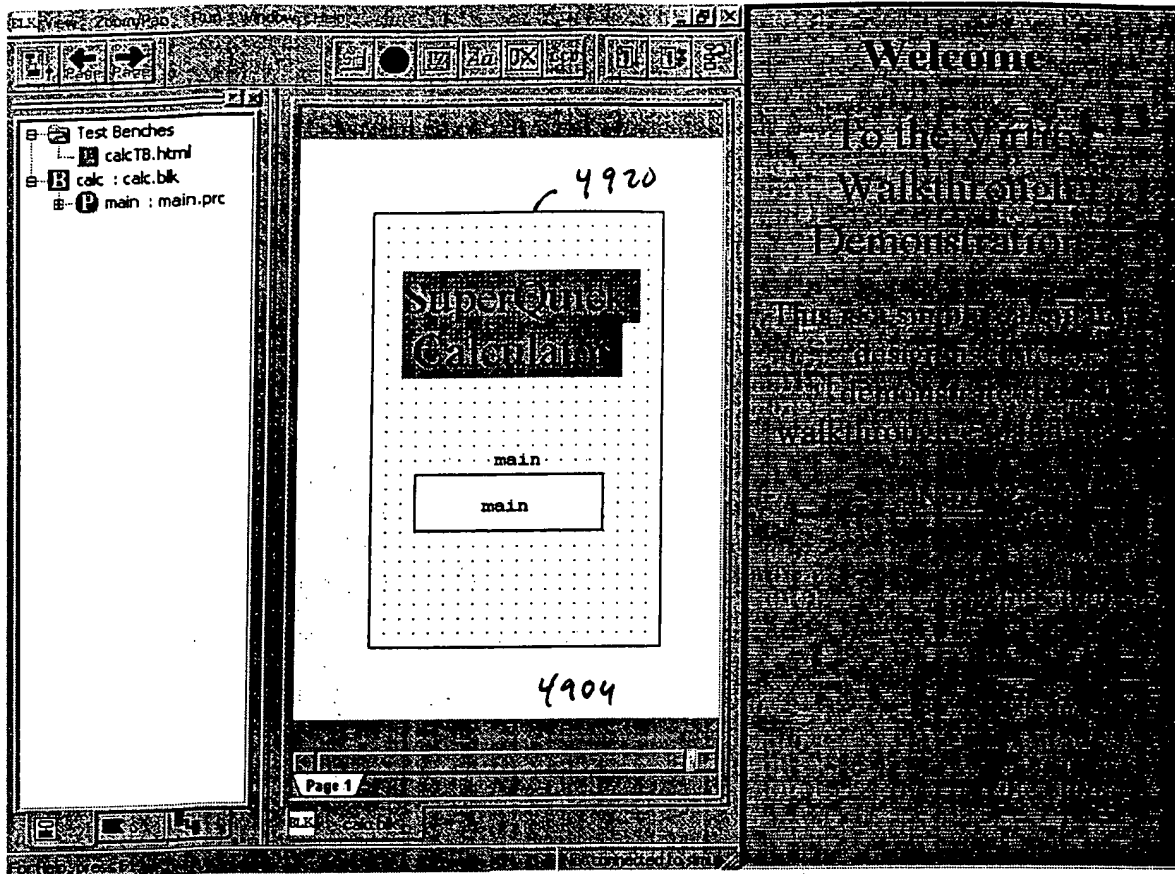
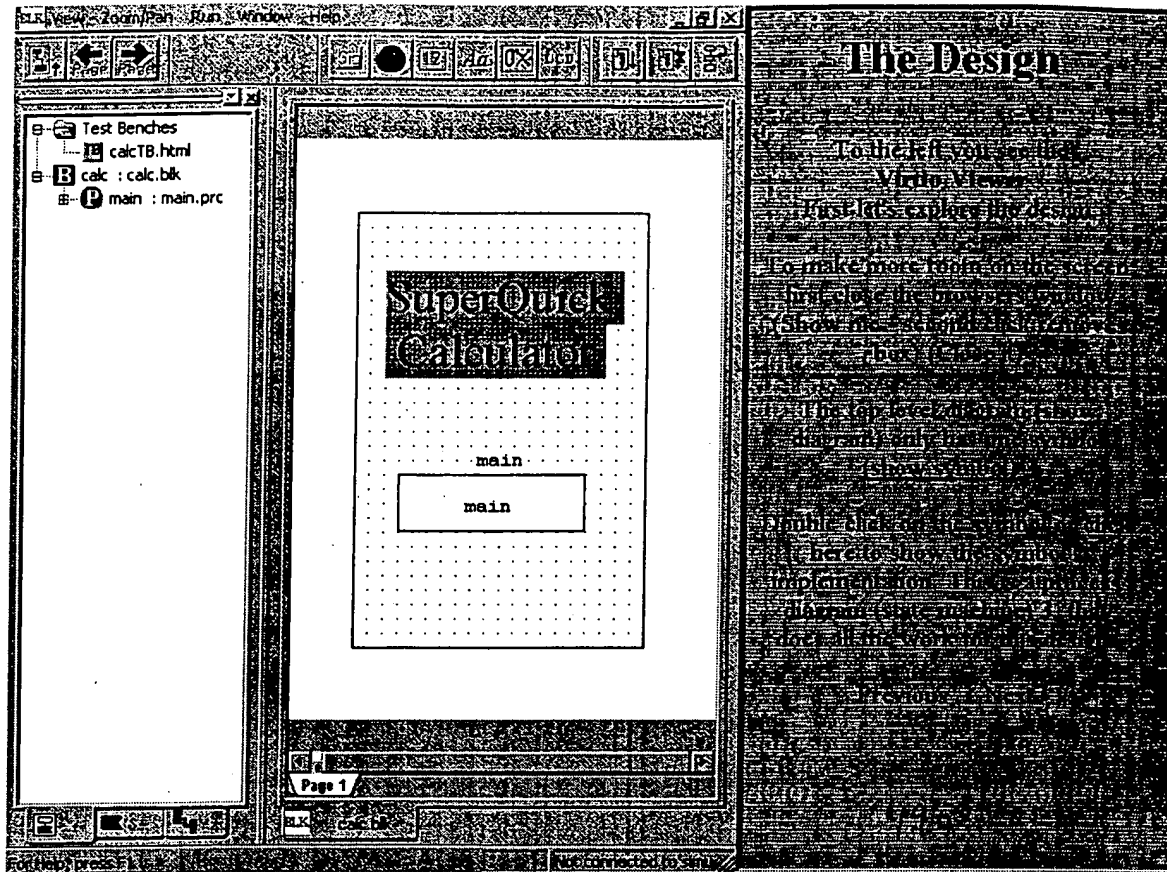
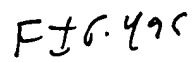


FIG. 49A



FI 6.49B





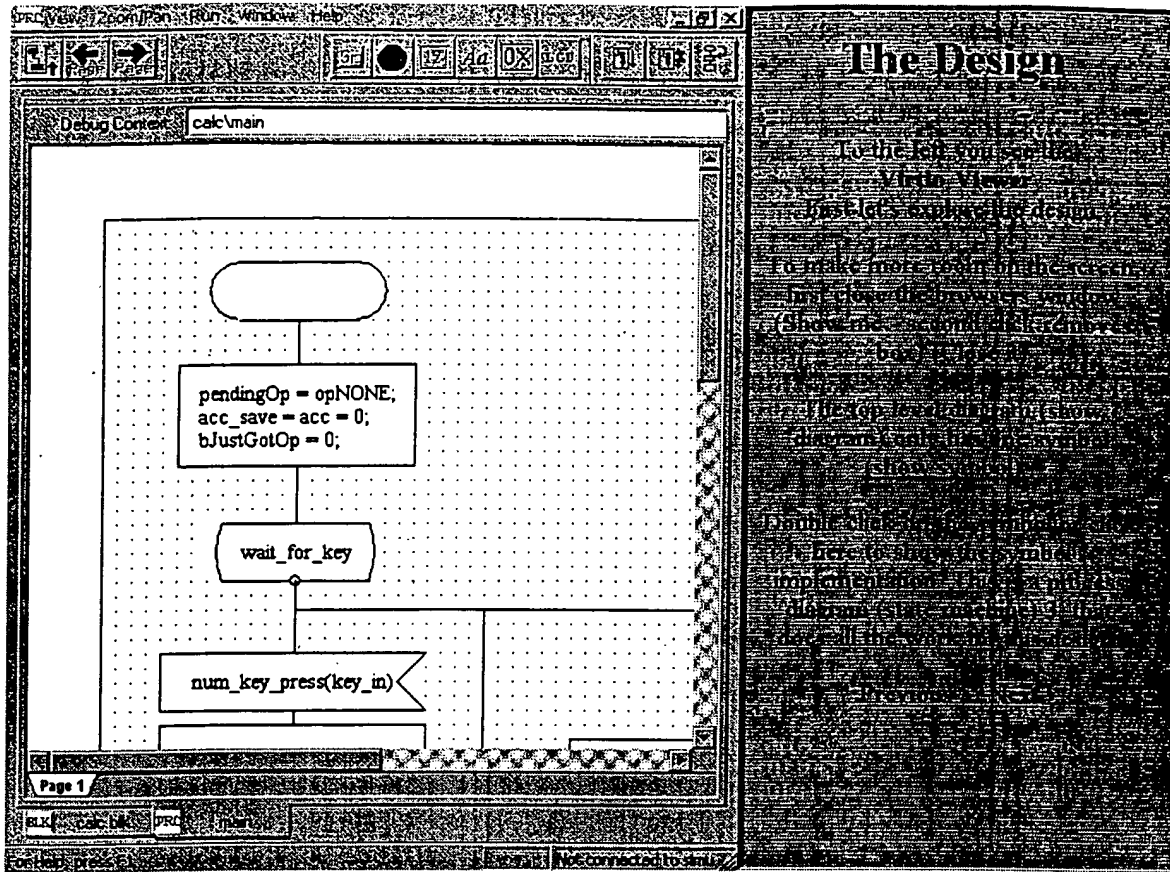


FIG. 49 D

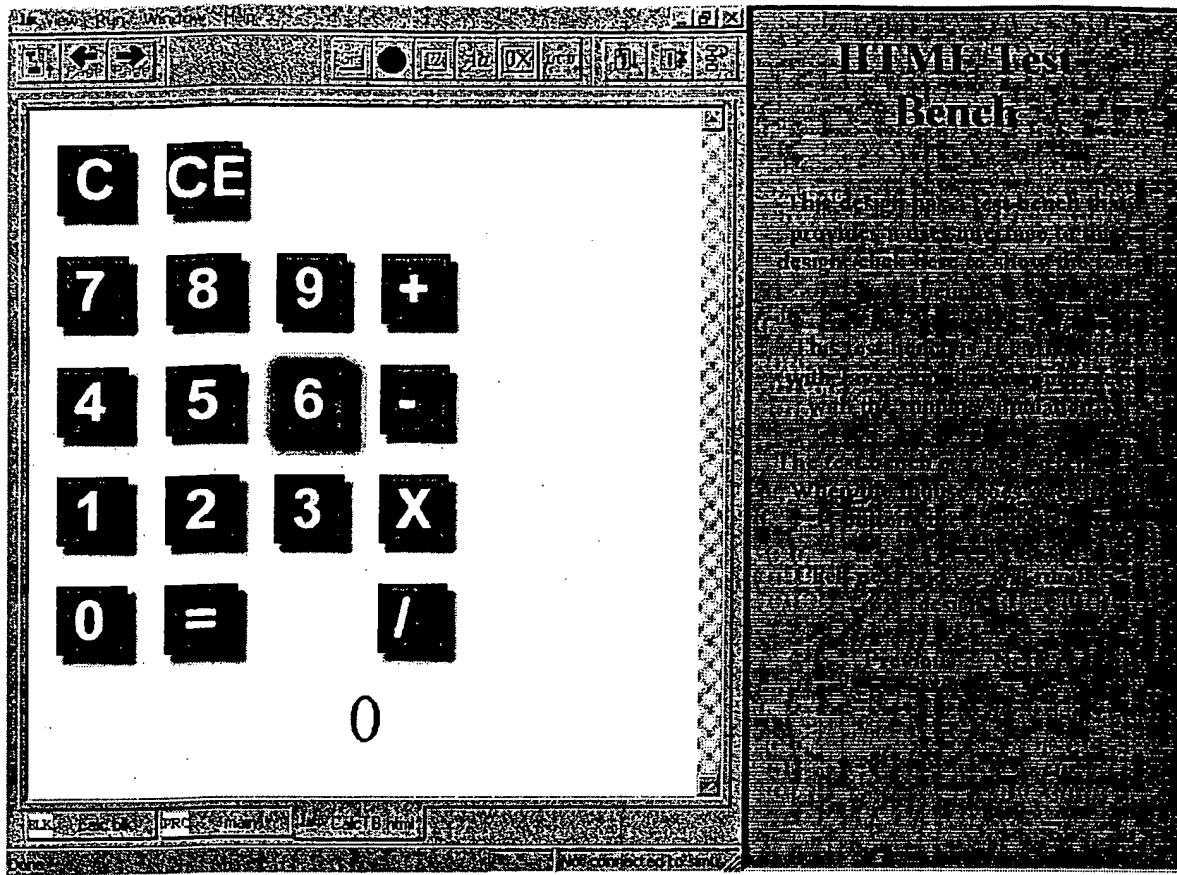


FIG. 49 E

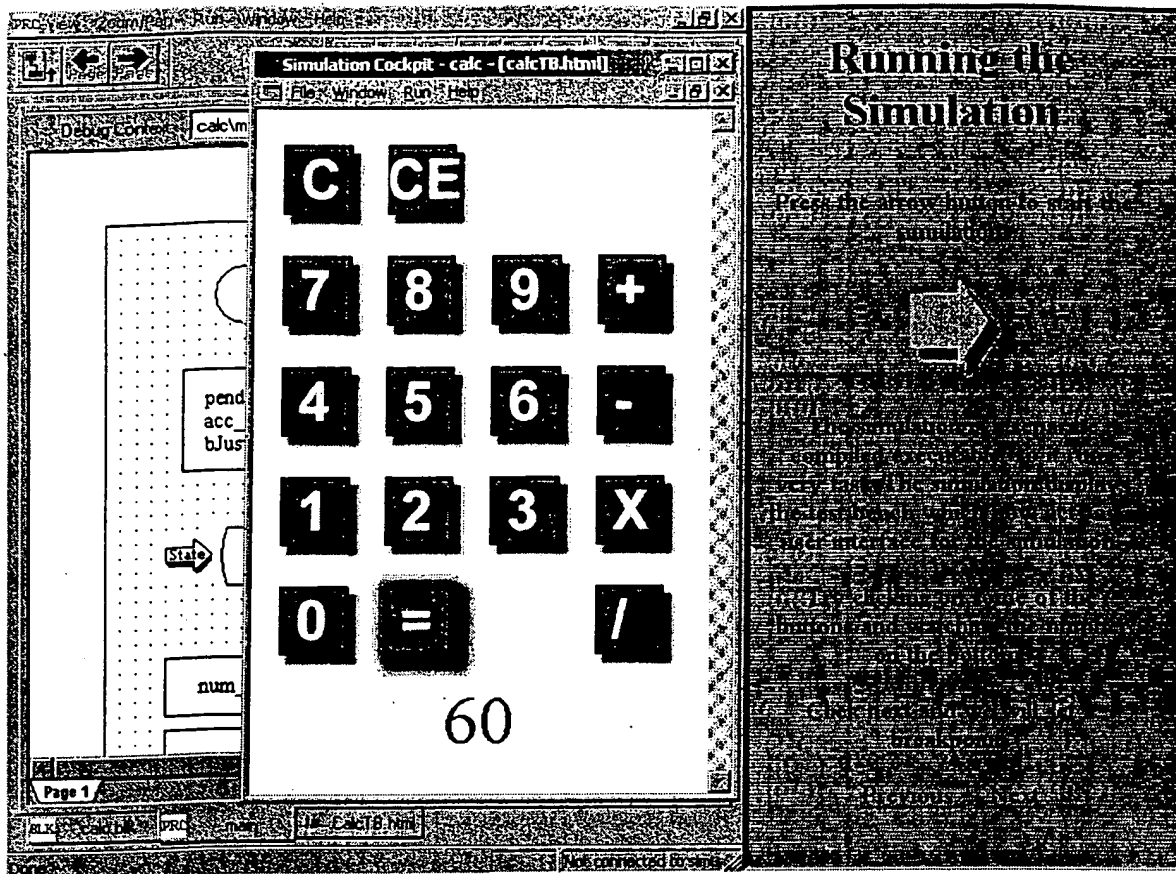


FIG. 49F

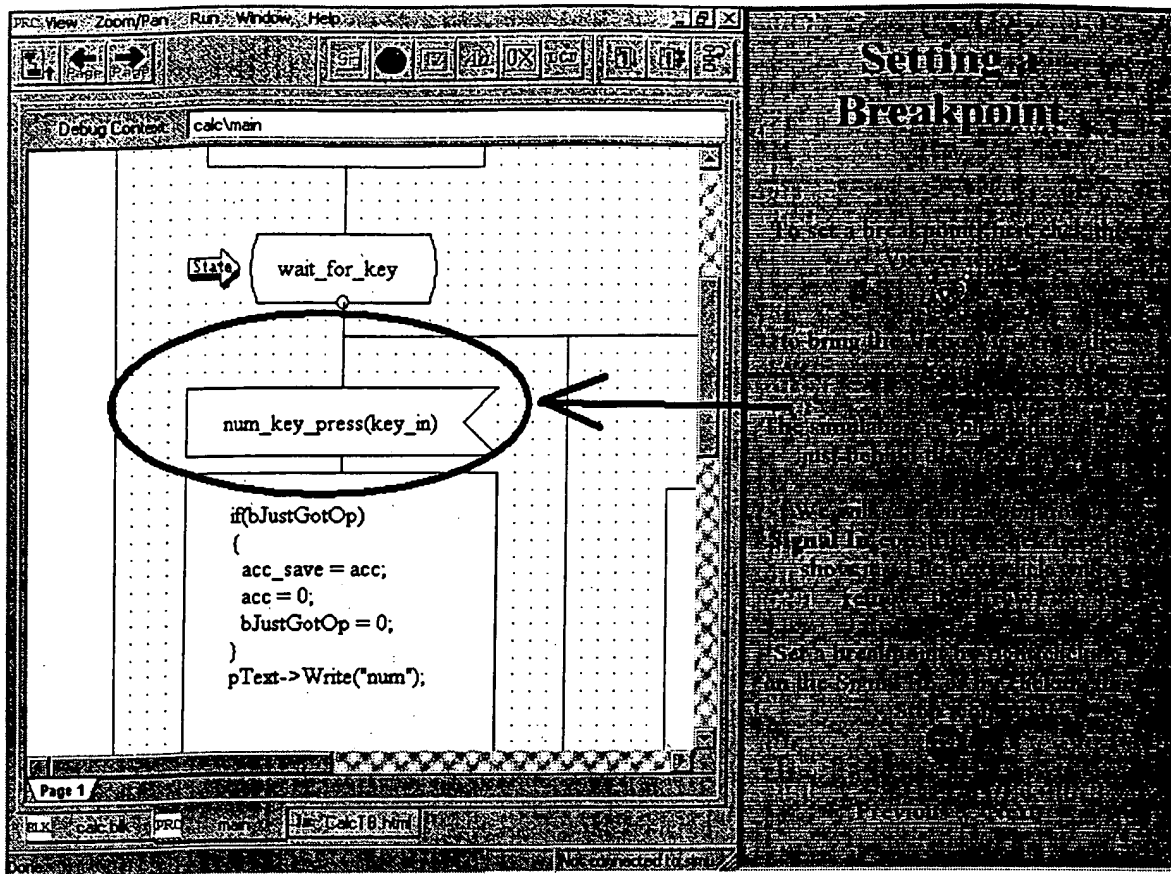
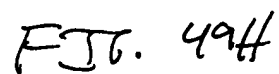


FIG. 49G



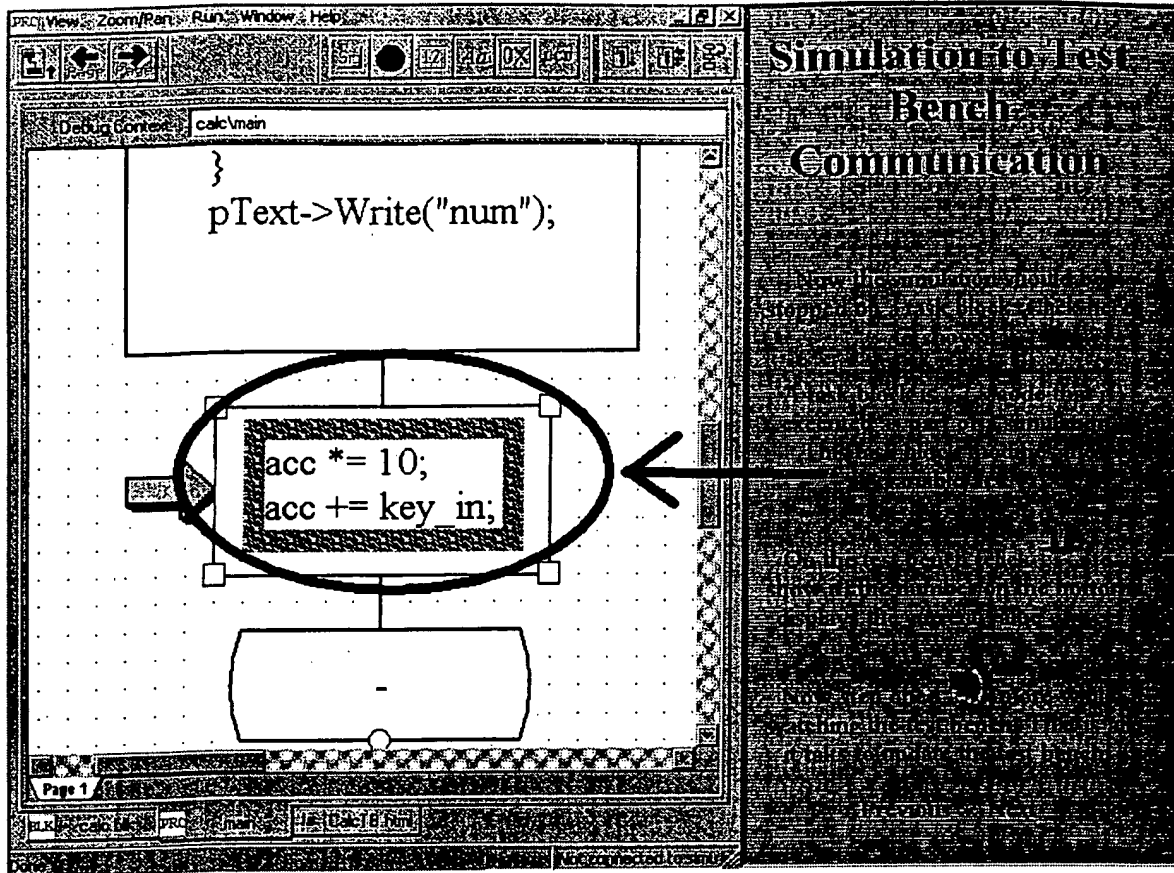


FIG. 49I

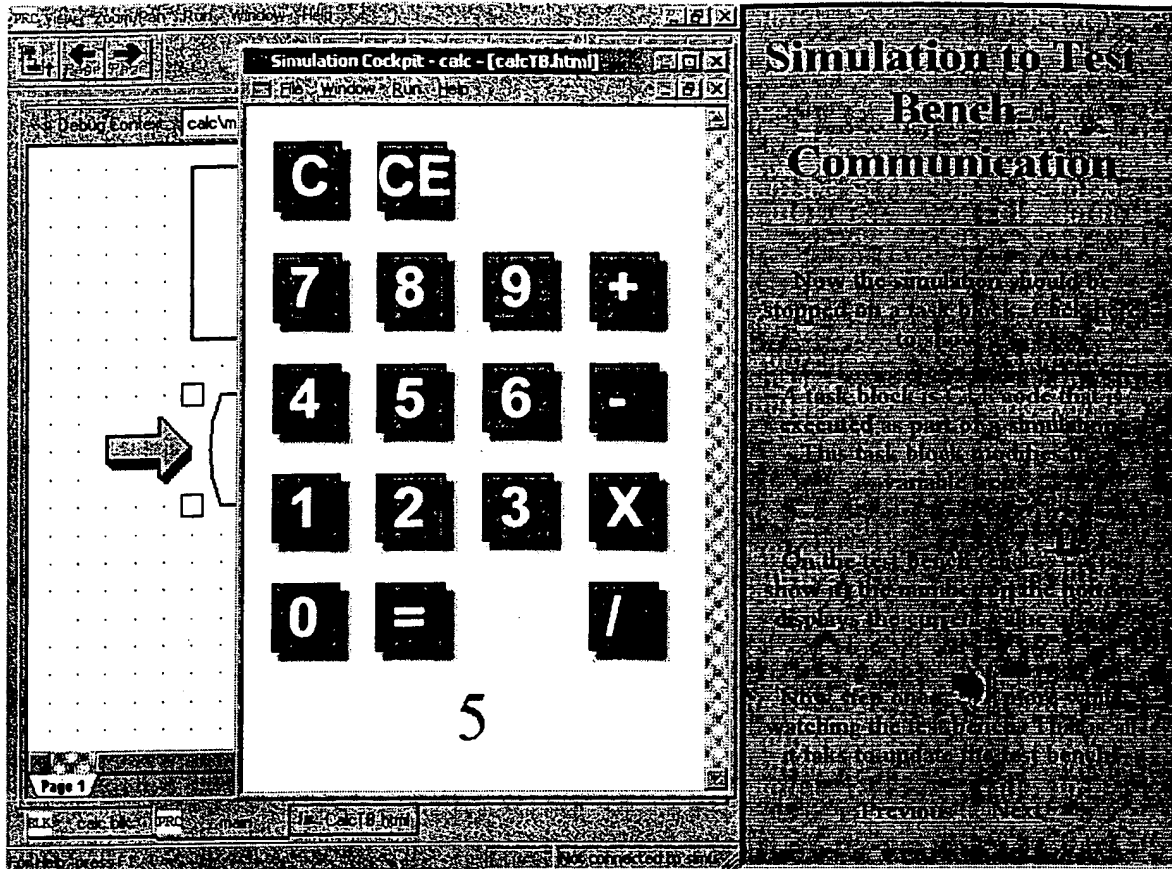
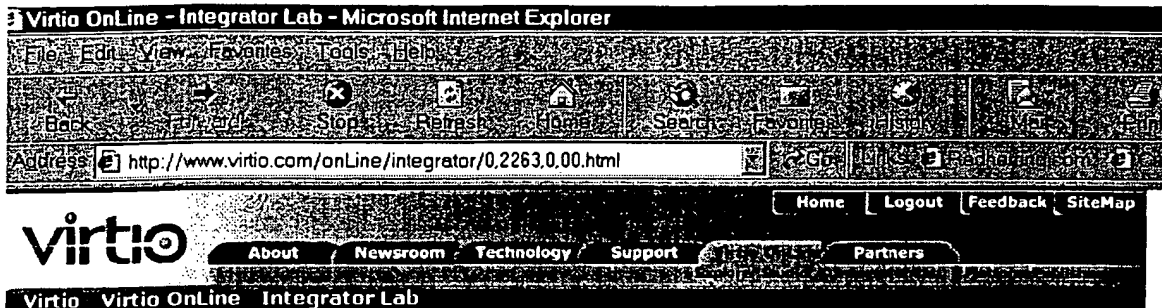


FIG. 49J

## Integrator Lab Screen Snap Shots – On-Line Enablement



### Integrator Lab

Current Designs				
Design Name ▼	Creation Date	Last Edit Date	Description	Delete Project
<u>test</u>	02-May-01	29-May-01	test	Delete
<u>pcnetlink</u>	04-May-01	25-May-01	asdasd	Delete
<u>clonetutorial</u>	23-May-01	23-May-01	testing cloning of build77	Delete
<u>clonehanoi</u>	25-Apr-01	31-May-01	cloning hanoi	Delete
<u>cloneatlas</u>	25-Apr-01	29-May-01	cloning atals	Delete

New Design


 My Invitees

FIG. 50



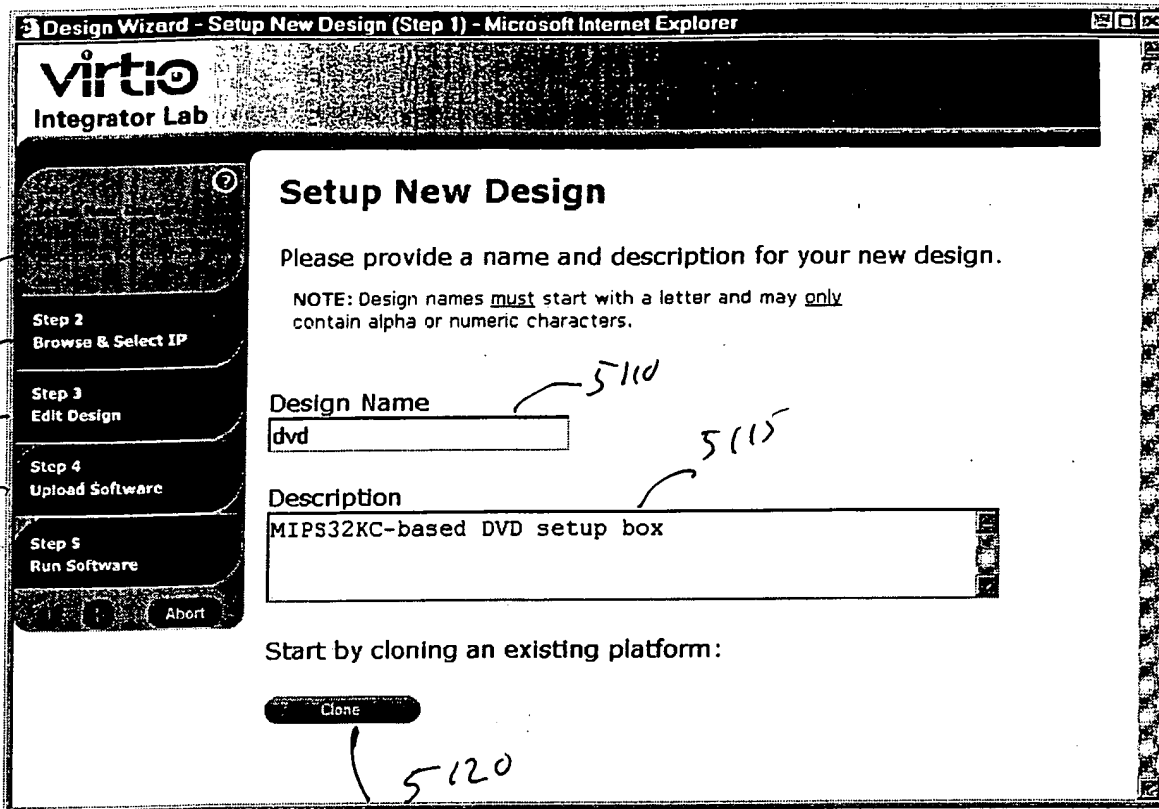


FIG. 51

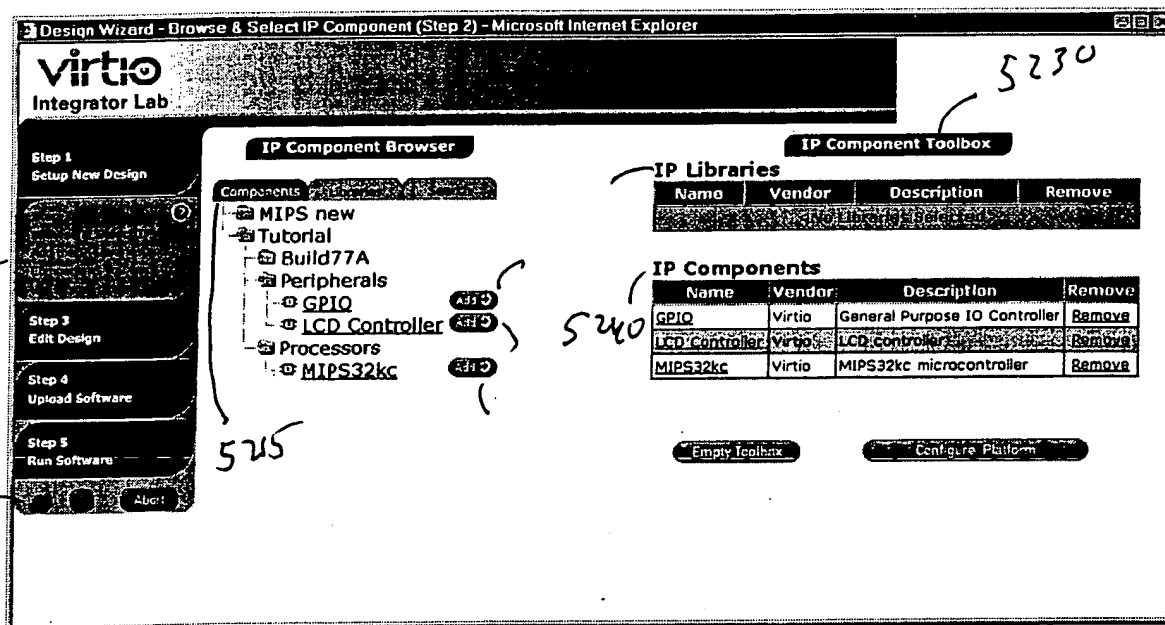


FIG. 52

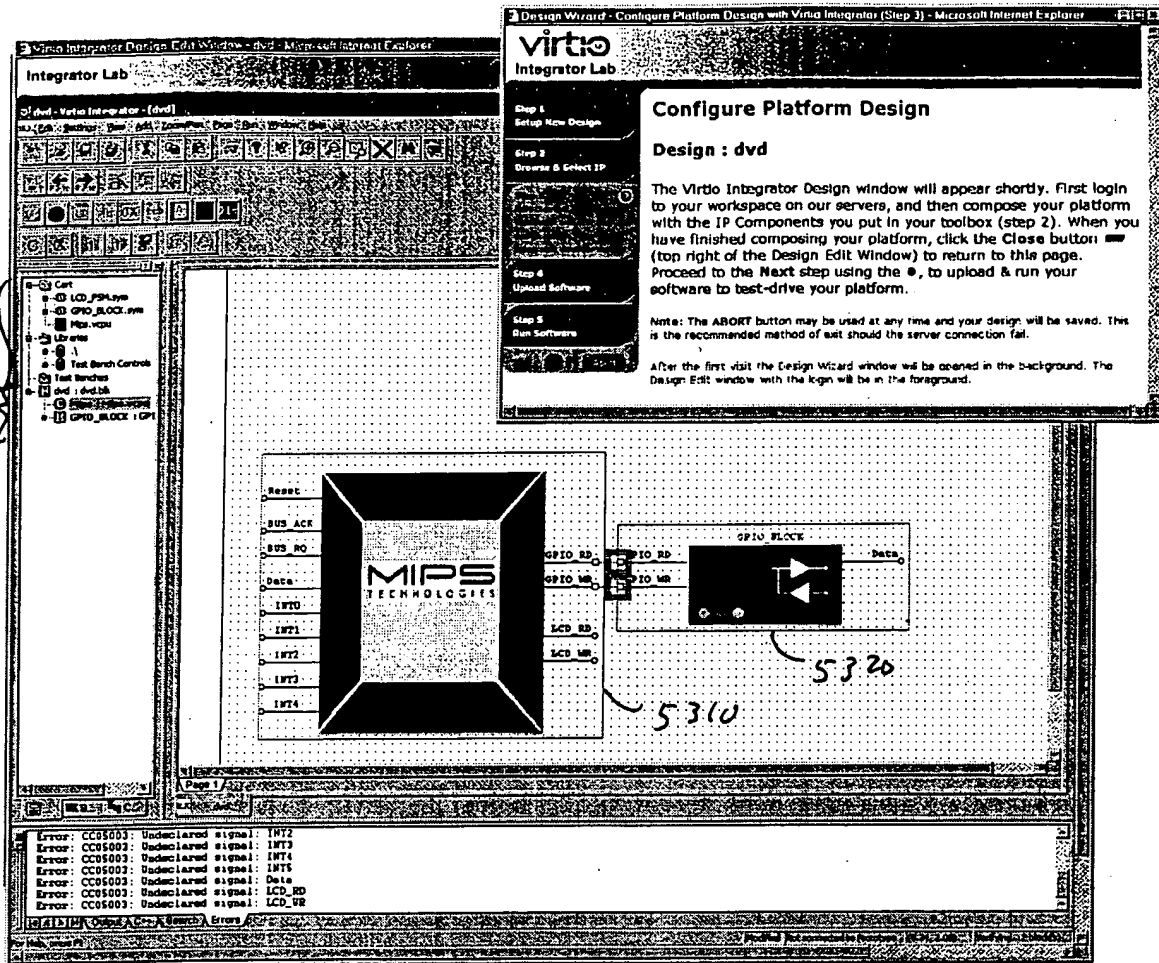


FIG. 53

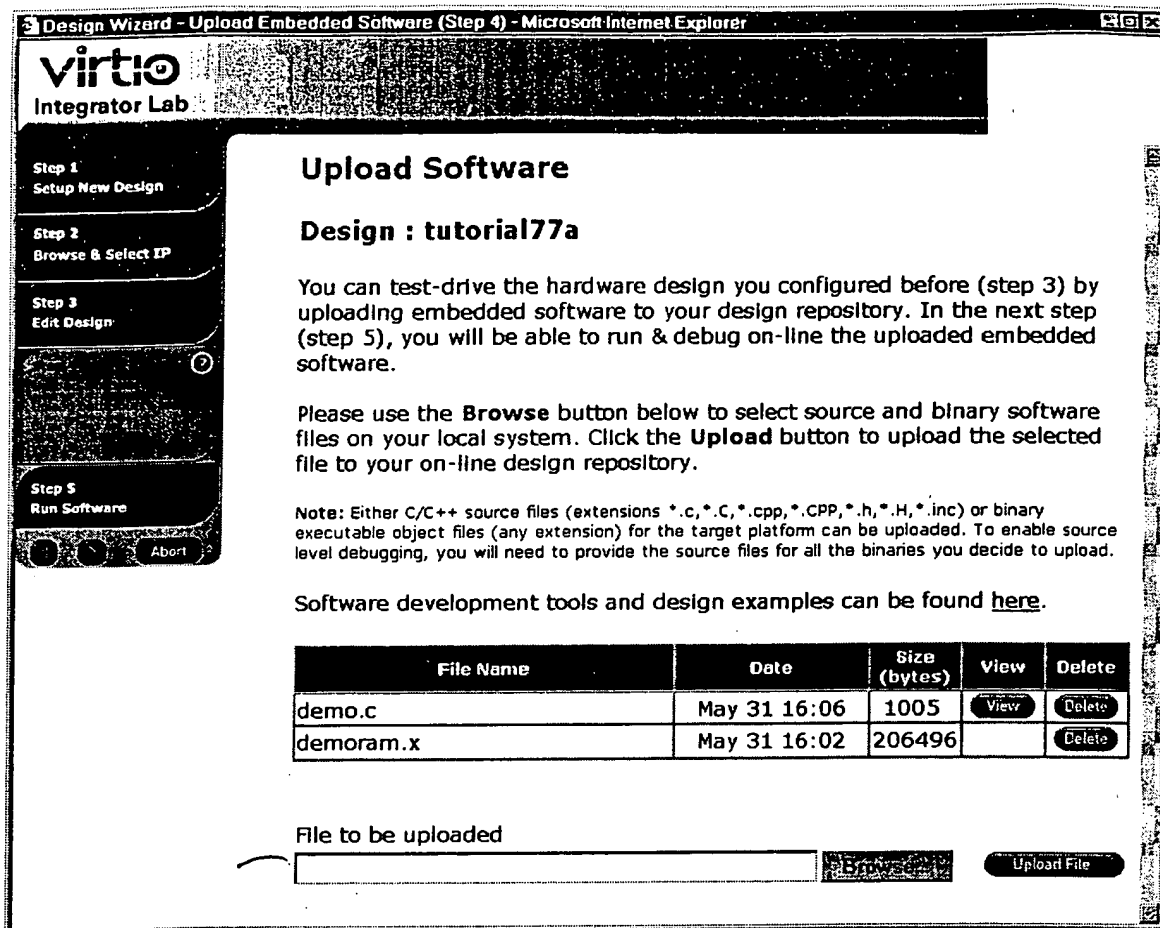


FIG. 54

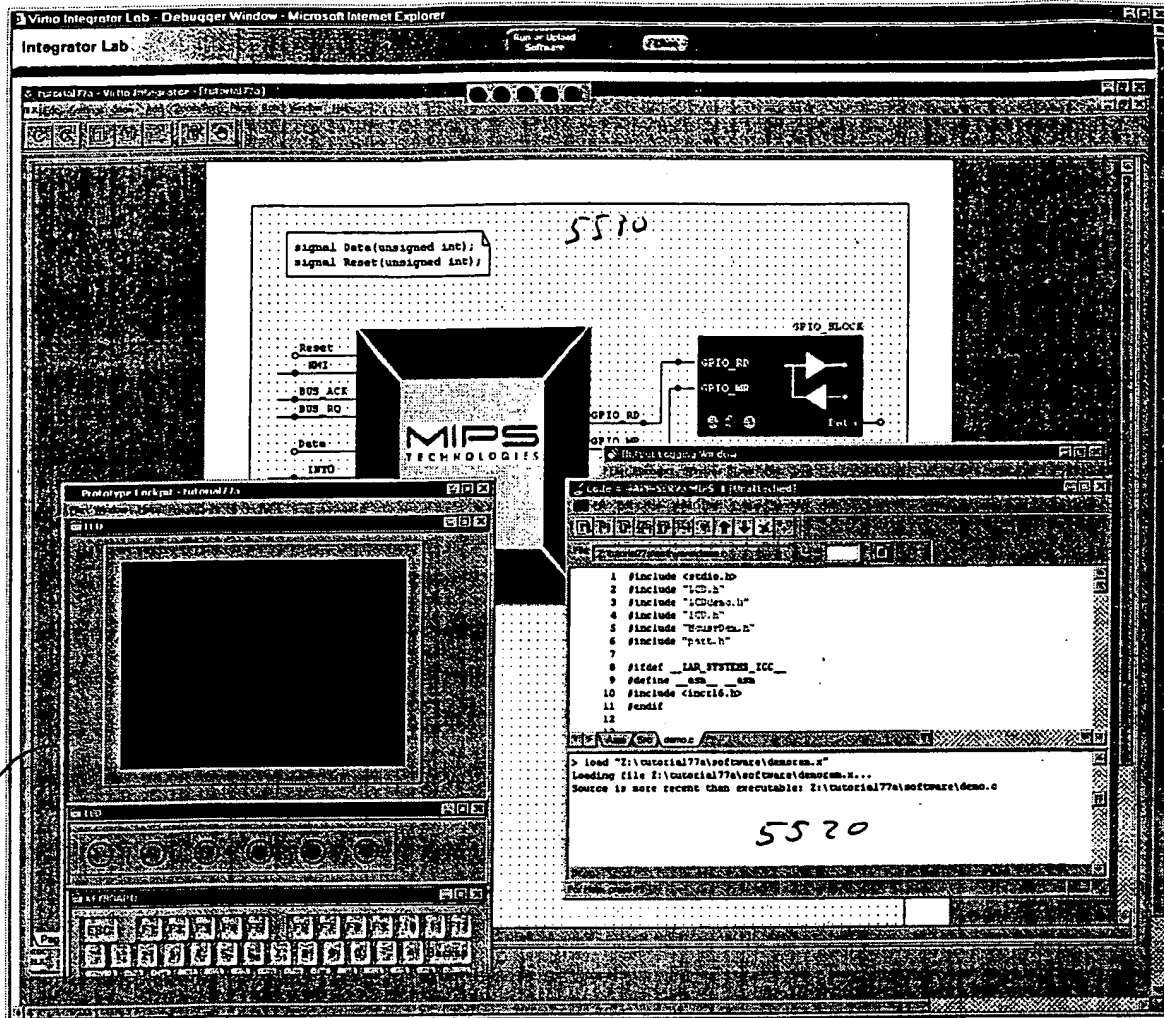


FIG. 55